Energy Conversion
Circuit Laboratory

공학박사 학위논문

태양광 패널 하드웨어 모사장치의 모델링과 안정도 해석 및 제어 기법 연구

Modeling, Stability, and Control for Solar Array Hardware Simulator

울산대학교 대학원

전기전자컴퓨터공학과

WELLAWATTAGE THUSITHA RANDIMA WELLAWATTA

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이 논문을 공학박사 학위논문으로 제출함

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UNIVERSITY OF ULSAN

Modeling, Stability, and Control for Solar Array Hardware Simulator

by

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Supervisor: Professor SUNG-JIN CHOI

A dissertation submitted in partial fulfillment of the requirements for

the Degree of Doctor of Philosophy

in the

Department of Electrical, Electronic and Computer Engineering

University of Ulsan

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I would like to dedicate this dissertation to my

beloved parents, my son, and my lovely wife:

Sarath Premalal Wellawatta

Koralagamage Padma Subhashini Weerawardhana

Eshya Wellawatta

Kariyapperuma Arachchige Nadeesha Chathurani

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Modeling, Stability, and Control for Solar Array Hardware Simulator

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Wellawattage Thusitha Randima Wellawatta

Submitted to the Department of Electrical, Electronic and Computer Engineering
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Abstract

Photovoltaic (PV) power generation has received renewed global interest from researchers worldwide as they are eco-friendly and readily available. PV systems are still undergoing significant changes, particularly in extracting maximum power from these modules at any given point. Maximum power point tracking (MPPT) algorithms emerged as a solution to extracting power at any instance. These algorithms need to execute to maintain the operating point on maximum power point. However, this cannot be accomplished under standard insolation and temperature conditions. A solar array simulator (SAS) scheme is demanded to address this, making it easy to incorporate varying temperature profiles and insolation levels while the same tests as many times as desired. PV systems exhibit a highly non-linear characteristic curve which makes simulation a challenge for researchers.

This paper is a stuy on modeling, system stability, and control method for a solar panel hardware simulator (Solar Array Simulator, SAS) used for the purpose of testing a photovoltaic system. The contents and contribution of this paper are as follows. same as

First, the stability of the control loop of the solar panel simulating device is structurally explained. First, in Chapter 2, the SAS system is classified mainly into a reference generator, a power stage and controller, and a load system connected to a photovoltaic panel replicator and modeled it. In particular, the reference generator is modeled and generalized using a super-ellipse approximation for convenience of analysis. The power stage is divided into constant resistance (CR), constant voltage (CV), and constant current (CC) loads, according to the type of load system. In Chapter 3, the SAS system is divided into the current control method (CRC) and voltage control method (VRC) in the primary control method, and voltage sensing (VS), current sensing (CS), and resistance sensing (RS) in the load sensing method. , the stability analysis is conducted for the type of load system as mentioned above. As a result, it is proved through theory and experiment that the resistance sensing voltage

reference control (RS-VRC) method is excellent in stability according to the operating point.

Second, a method for extending the operating range of the SAS system is proposed. In the solar I-V curve, when the operating point moves to the open-circuit voltage and short circuit current regions, the voltage control method and the current control method have advantages, respectively, so a hybrid control method selects two or more different controllers are used. In this case, mode switching occurred, and there is an issue in that the response characteristics deteriorated. To supplement this, the MRS-VRC and MRS-CRC methods are proposed as a modified resistance sensing (MRS) method that adds an offset voltage and current by modifying the resistance sensing method, and the improvements are verified through simulation and hardware.

Third, in order to prepare for a case where a rapid operating point change is necessary, a high-speed reference generation algorithm is studied. In the diode equivalent model equation of a solar panel, which is mainly used in past studies, the current-voltage relational expression appears in the implicit form. To generate the reference, an iterative algorithm is used, or a look-up table is generated. However, the Lambert-Ω function, which changes it to an explicit form, has been proposed. However, since the Lambert function also uses iterative calculations, the speed is not fast, so in this paper, a solar panel reference generation method using the approximate Lambert function is proposed. In addition, for a more simplified analysis model, a super-ellipse approximation is proposed in this paper, and its accuracy was verified to be relatively good. This model is used for stability analysis in Chapters 2 and 3 of this paper because the equations are quite simple. On the other hand, as a power stage circuit to solve the problem of rapid load change, especially the voltage reduction time delay caused by the output capacitor, a bidirectional converter structure is proposed instead of the conventional unidirectional converter structure, and its performance is verified by simulation.

Through the above research, it is expected that the SAS system can be made more robust to changes in load or insolation by establishing a method for improving the stability of the SAS system, increasing the operating range, and establishing a high-speed control method.

Thesis Supervisor: Sung-Jin Choi
Title: Professor

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Chapter 1

Introduction

1.1 Overview

All over the world, solar power is the most readily available and safe renewable energy source with numerous advantages, including; non-particle (or low-carbon) emission, quietness, durability, and low maintenance cost. Over the years, various research has been conducted to enhance the role of photovoltaic power in fulfilling current energy demands while preparing for the future. Thus, the research related to the photovoltaic (PV) application conducts numerous roles for future power generation in human civilization. However, the current level of technology and market trends of the PV industry is not enough to fulfill future energy demand, reflecting the need for more research and developments.

Generally, PV systems have three main sections based on their function: energy harvesting, power conversion, and energy-storing or utilization. The energy harvested by PV cells is fed into the power conversion system (PCS). This section evaluates the PV array characteristics and establishes interconnection with the load (such as battery systems or microgrids). The power conversion system should maintain an appropriate current and voltage ratio (determined from the PV array characteristics) at all times required to obtain the maximum power point (MPP).

The value of MPP at any instant is dependent on numerous factors such as the structural properties of the PV module, insolation level, and module temperature. Nonetheless, PCS usually receive the largest buck of input from the PV array. The voltage and current values serve as the intake and are used as sensing data for determining the current MPP. This tracking is achieved with the aid of various kinds of maximum power point tracking (MPPT) algorithms incorporated with the power converter (i.e., DC-DC or DC-AC converter). The

PCS is divided into two segments; an MPPT system and a power converter.

For PV systems, a well-controlled PV array is of utmost importance as the PCS will operate under varying conditions, including PV panel material, array architecture, insolation level, and temperature conditions. Under ideal conditions, this can be an unfeasible task due to the repetitive patterns observed in insolation and temperature levels. A solar array simulator (SAS) concept is used to address this requirement, which provides many user-determined parameters such as insolation and temperature patterns, steady-state and dynamic conditions, configurable array architectures, selection of PV brands and models, and data logging features. Due to non-linearity and variation in the load, implementing the PV characteristic curve and PV characteristic equation of SAS can be quite a challenge, increasing system complexity. Under the minimum condition, the worst-case scenario of the PV curve should be considered, and this is known as the MPPT standard test procedures such as EN50530 [10]. It is worthy to note that there is no known standard pattern for varying the load yet. MPPT algorithms often require a SAS response speed that is at least five times faster than its own speed [11–13], making the global MPPT algorithm. This means the SAS often needs high-speed and accurate controllers. one of the commercial SAS is shown in Fig. 1-1. Consequently, different types of approaches for the SAS are discussed in the literature [14, 15].

SAS has three subsystems: the PV reference generator, hardware controller, and DC-DC converter, as shown in Fig. 1-2. The SAS reads the required input parameters such as insolation and temperature profile, output voltage, and current and generates the required reference signal for the DC-DC converter controller. This process can be achieved by using the characteristic equation or data manipulation from a large amount of pre-recorded data table in the PV reference generator. The controller follows the reference signal with feedback from the converter output, which produces the DC-DC converter control (duty) signal, thereby controlling the output, the PCS input. This ensures that the SAS output becomes directly emulates the characteristic of the target PV system.

1.2 PV module characterization

The components of photovoltaic collectors can be defined as main four terminologies as shown in Fig. 1-3 according to [16]. The unit element of the photovoltaic component can be identified as the solar cell (PV cell). It is made by a P-N junction formed by a specific

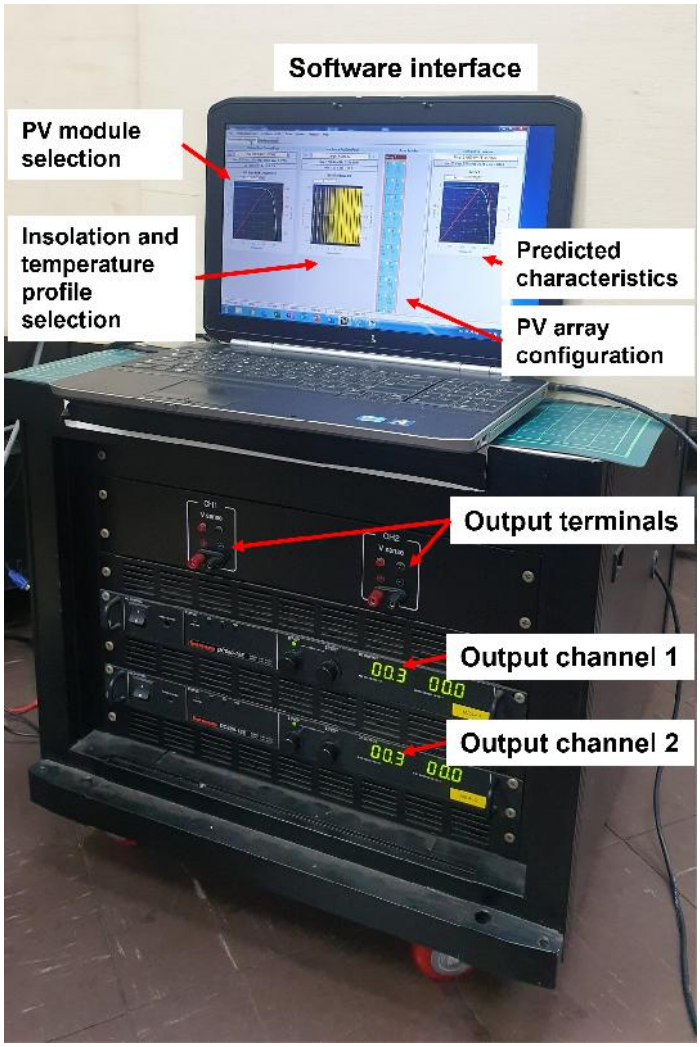


Figure 1-1: Commercial SAS system (TerraSAS)

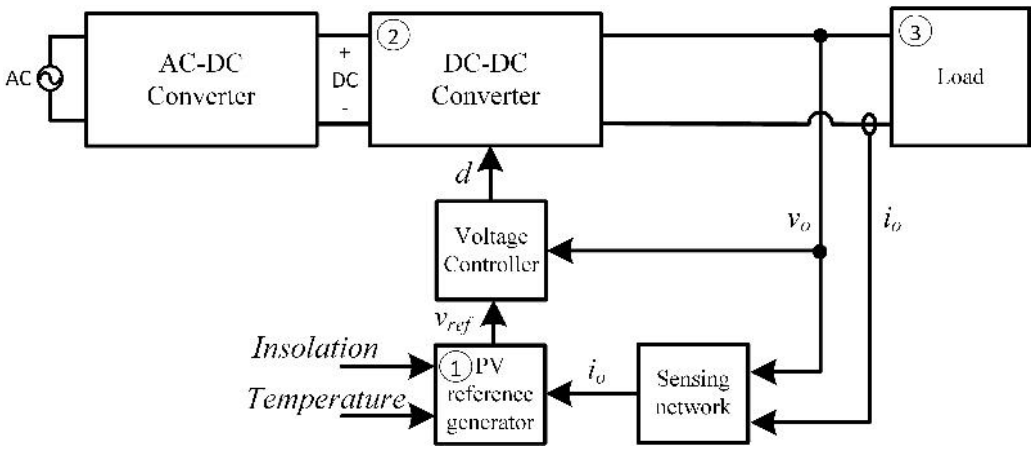


Figure 1-2: Typical SAS system

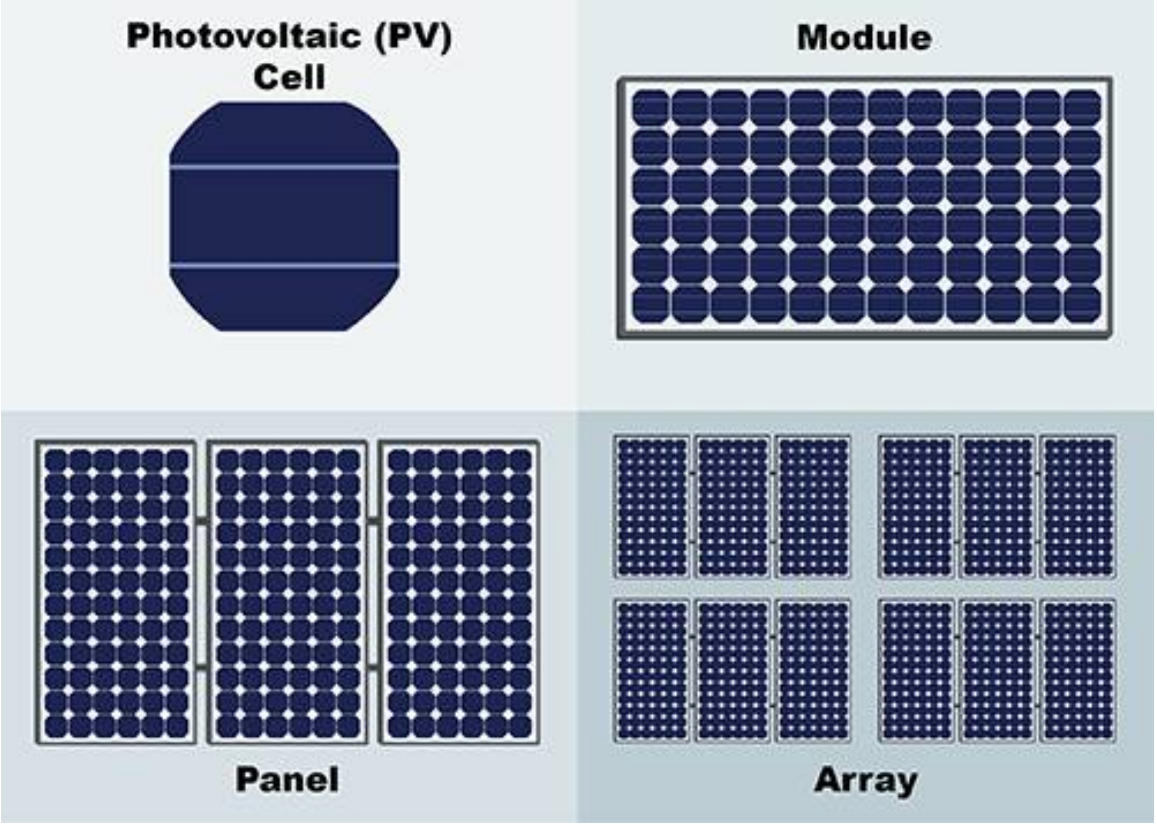


Figure 1-3: Classification of PV component

process. By series or parallel connection of PV cell, PV module is constructed. Usually, a bypass diode is connected to the terminal of the PV module to protect it from reverse voltage. A few PV modules can be fixed into one frame to have the mechanical weight balance, which is called a PV panel. Such panels are connected as a PV array using desired configuration [17] in PV farm.

In an illuminated solar module, a specific photovoltage is generated relevant to a photocurrent. That current and voltage are known as operating points and determined by the insolation and temperature of the PV module, PV characteristics, and the load resistance R_L. Behavior of v_{pv} vs R_L can be plotted as R-V curve as shown in Fig. 1-4. According to R_L curve, the PV voltage is very low at lower R_L, and the PV current is very low at very high R_L. Thus, the short circuit current(I_{sc}), open-circuit voltage (V_{oc}) of a solar cell are defined as a R_L which is equal to zero or which is infinitely high, respectively. The I–V characteristic curve of a solar module can be identified as a graph of all operating points in a treated range. The P-V curve also demonstrates the PV module behavior, and that I–V and P-V characteristic curves are shown in Fig. 1-5. By the P-V characteristic, a critical point has its maximum power, which can be identified as a peak of the curve. The voltage

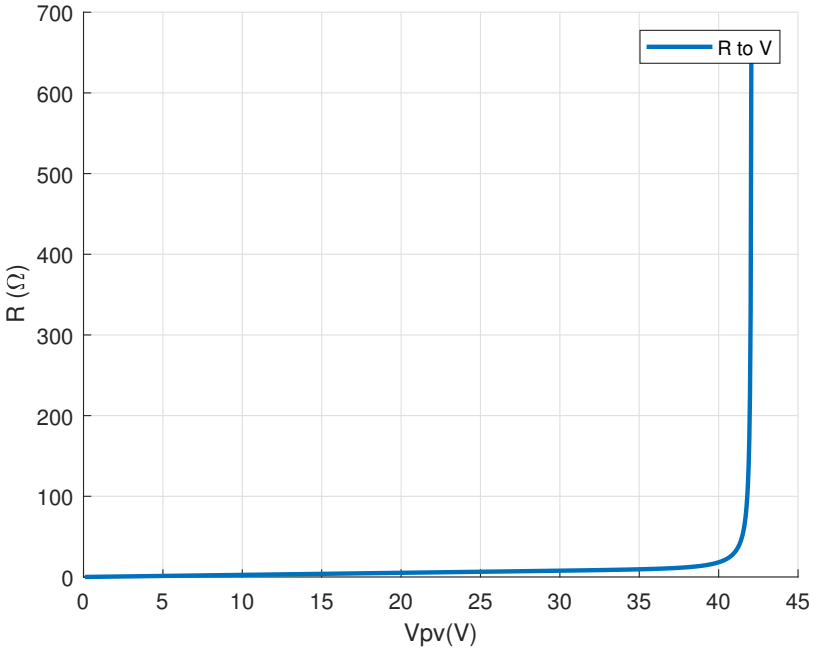


Figure 1-4: R-V characteristic curve of PV module

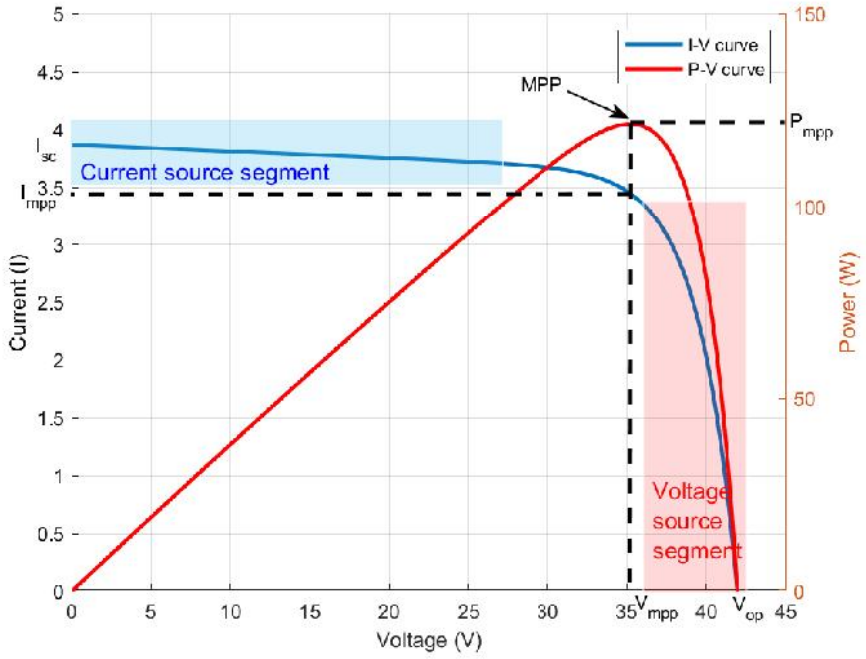


Figure 1-5: I-V and P-V characteristics curves of PV module

of this peak is known as V_{mpp}, and the relevant current of the I-V curve is known as I_{mpp}. This point (V_{mpp}, I_{mpp})is called the maximum power point (MPP), and the maximum power P_{mpp} can be calculated as

$$P_{mpp} = I_{mpp}V_{mpp}. \tag{1.1}$$

The values of I_{sc} and V_{oc} can be measured by opening and closing the PV module terminal. Thus, those operating points are taken to characterize the solar module. That points and MPP (V_{mpp},I_{mpp}) can be used for the reconstruction of any PV module. Additionally, the product of I_{mpp} and V_{mpp} has a relation to the product of I_{sc} and V_{oc}. This parameter demonstrates the amount how much the rectangle of V_{oc}, I_{sc} is filled by the rectangle of V_{mpp},I_{mpp} and thus is known as the fill factor (FF).

$$FF = \frac{I_{mpp}V_{mpp}}{I_{sc}V_{oc}} \tag{1.2}$$

The fundamental characteristics of the PV module can be understood by considering the physical structure of PV cells. PV modules are available as the smallest physical PV unit in the market.

Let us consider that a PV junction is in a zero insolation atmosphere. When a voltage source (U) is connected to junction terminal, the diode is forward biased as shown in Fig. 1-7a and its equation can be written as . The diode saturation current (I_s) is dependent on the material and physical geometry of the PV cell. However, when the voltage source is removed and the P-N junction is exposed to light, as shown in Fig.1-6 [1]. It makes a current source in the depletion layer with the direction of diode reversed bias according to the photocell phenomena, and it causes the produce diode barrier voltage itself. If there is no external close circuit, this current is sunk as a forward bias current of the diode as shown in Fig. 1-7b. When considering the diode characteristic curve, this effect can be understood as curve shifting towards the negative current direction as shown in Fig. 1-8 [2].

$$I = I_D = Is\left(e^{\frac{U}{AV_t}} - 1\right) \tag{1.3}$$

The characteristic equation of this case can be derived as

$$I = Is\left(e^{\frac{U}{AV_t}} - 1\right) - I_{PH} \tag{1.4}$$

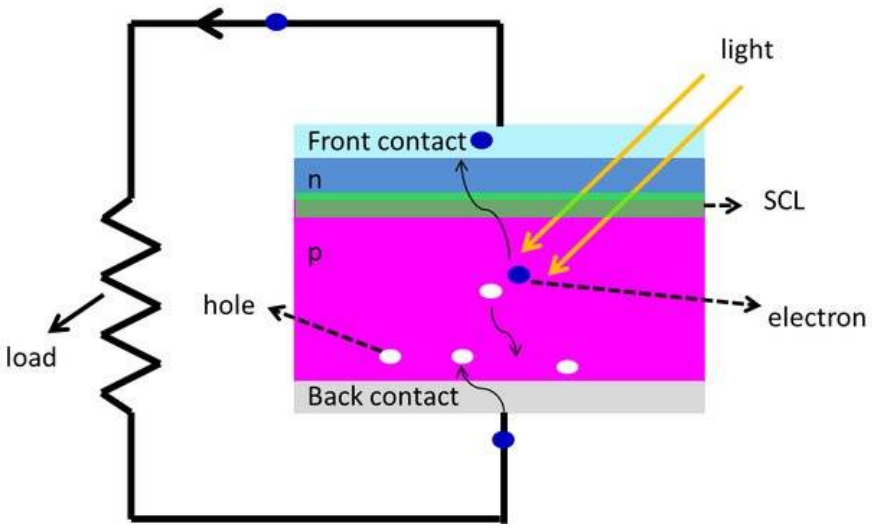


Figure 1-6: pn junction solar cell [1]

In the case of the actual PV cell, it has added two parasitic resistance, which is serially affected to the current flow (R_s) and leakage resistance paralleled to the current source (R_{sh}). It can be modeled as shown in Fig. 1-7c and the model equation can be derived as bellow. Here, the I_D should be modified according to the voltage drop of the R_s.

$$I = I_s \left(e^{\frac{U - IR_s}{AV_t}} - 1 \right) + \frac{U - IR_s}{R_{sh}} - I_{ph} \tag{1.5}$$

This P-N junction with R_s and R_{sh} is known as PV cell, and voltage "U" is known as V_{PV} and load resistance is connected to the PV terminal. The usable current flow is usually taken in the opposite direction of the "I." Thus, (1.5) can be multiplied by -1, and "-I" can be taken as I_{PV}. Then, the equation 1.6 in can be obtained, and by mirroring the PV diode characteristic curve through the voltage axis, a general PV I-V curve can be obtained. PV cells are connected as an array, and PV modules are fabricated and available in the market. In that case, individual cell voltage and currents are added according to the cell array pattern and become specified ratings.

As explained above, when the P-N junction is exposed to atmospheric light through the transparent glass, this energy dislodges an electron and creates a free electron and hole, which is the opposite of the principle of operation of a light-emitting diode (LED). Due to the electric field of the depletion layer, free electrons and holes are forced into the N-region and P-region, respectively. That causes to increase in the junction voltage, P-region (anode) as positive, and N-region as negative (cathode). Fig.1-7d shows exponential I-V

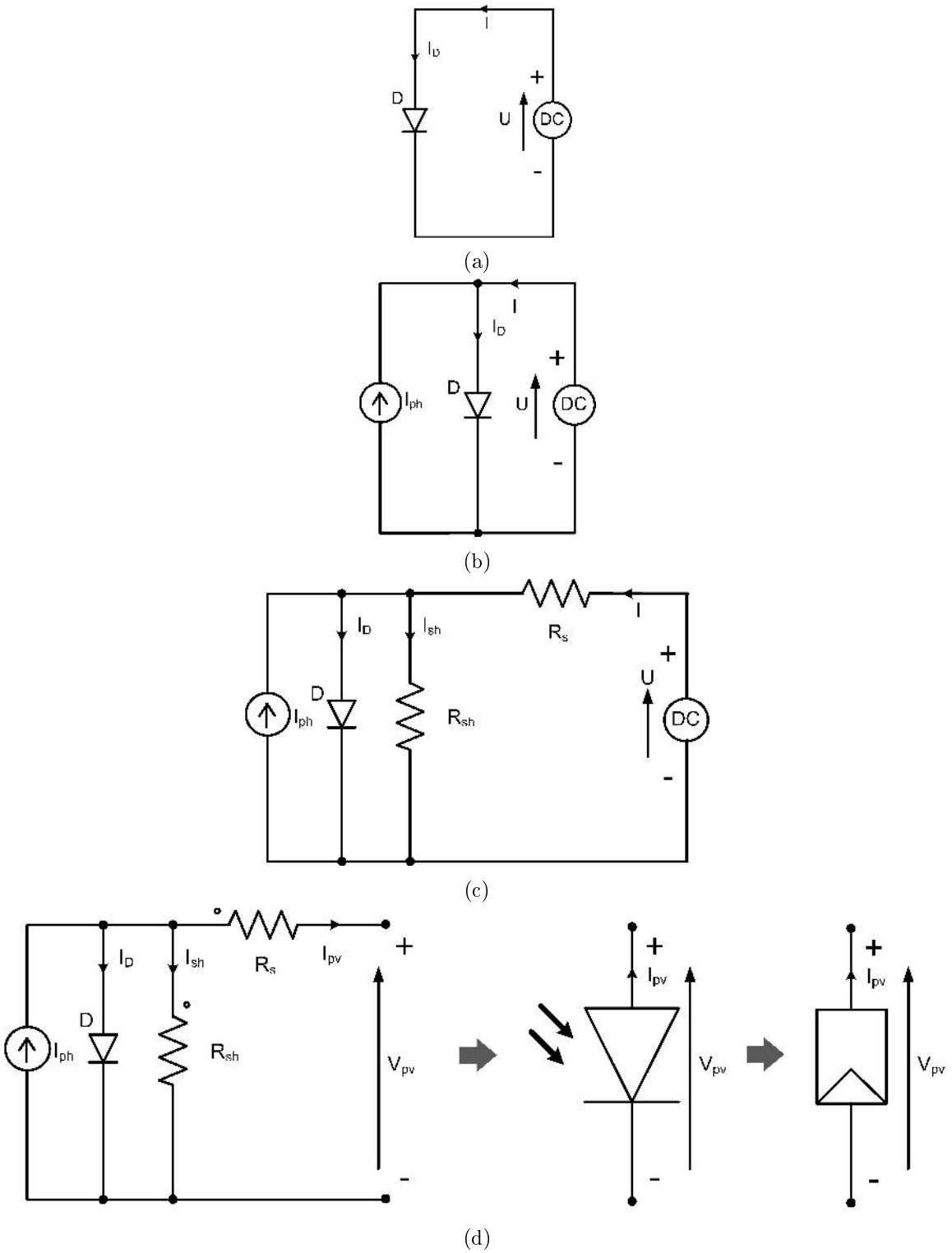


Figure 1-7: Development of PV model as a modification of junction diode (a)Forward bias condition of P-N diode (b)Ideal PV cell under insolation (c) PV cell with parasitic resistance (d) Equivalent circuit of PV module

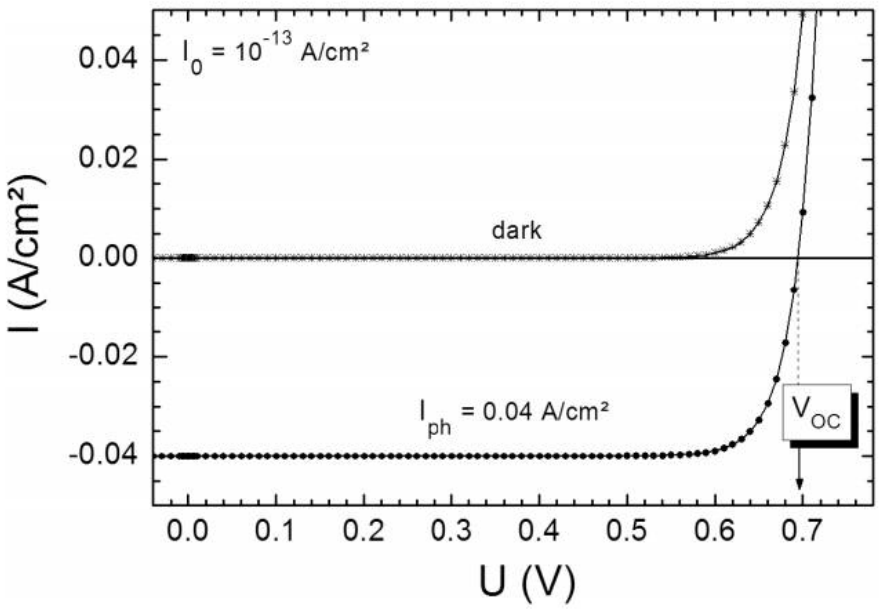


Figure 1-8: I-V characteristics curve PV cell as a diode [2]

characteristics; also, the most popular equivalent circuit model of PV can be identified as depicted in Fig. 1-5. However, this characteristic equation becomes implicit as in 1.6.

$$i_{pv} = I_{ph} - I_s \left[e^{\left(\frac{v_{pv} + i_{pv} R_s}{A N V_t} \right)} - 1 \right] - \frac{v_{pv} + i_{pv} R_s}{R_{sh}} \tag{1.6}$$

where i_{pv} is the module output current (A), I_{ph} is the photovoltaic current (A), I_s the saturation current of the diode (A), v_{pv} is the module output voltage (V), V_t is the thermal voltage (V), A is the ideality factor, R_s is the series resistance (Ω), R_{sh} is the parallel resistance (Ω) [18], and N is the number of series cells in the module. V_t can be further demonstrated as

$$V_t = \frac{k\theta}{q_e} \tag{1.7}$$

where k is the Boltzmann constant, θ is the absolute temperature of PV string in Kelvin, and q_e is the charge of electron ($1.602 \times 10^{19} C$). The I_{ph} is dependent on the insolation and temperature. It can be calculated as

$$I_{ph} = I_{scn} \frac{\phi}{\phi_{STC}} + C_t(\theta - \theta_{STC}) \tag{1.8}$$

where I_{scn} is the short circuit current at STC(Standard Test Condition: $\theta_{STC} = 298.15K$ temperature,$\phi_{STC} = 1000W/m^2$ insolation), θ is the module temperature in Kelvin, ϕ is

the module insolation, and C_t is the temperature coefficient of I_{sc}. The I_s is dependent on the temperature and can be calculated as

$$I_s = I_{scn}\left(\frac{\theta}{\theta_{STC}}\right)^3 e^{\frac{q_e E_g}{AK}\left(\frac{1}{\theta_{STC}}-\frac{1}{\theta}\right)} \tag{1.9}$$

where E_g is the band-gap energy of the module.

As shown above, the value of I_{ph} is dependent on the insolation and temperature of the PV module. Assume the R_{sh} is close to infinity for simplification, in the no-load case, the equivalent diode sinks most portion of I_{ph}, and the forward voltage drop can be considered as open-circuit voltage (V_{oc}). In the short circuit case, the I_D becomes zero, and most I_{ph} passes through the load as a short circuit current (I_{sc}).

Thus, the maximum power can be extracted from the PV when the load resistance gets nearly equal to the Thévenin's equivalent resistance of the PV [19].

1.3 Typical SAS system structures

The basic block diagrams of each system are shown in Fig. 1-9, and it contains voltage or current controller with four PV reference generation schemes. In the literature, most studies can be categorized into those basic configurations and can be classified according to the Table 1.1. Feedback control loop inside SAS consists of inner loop and outer loop configurations, and some studies proposed different system analysis techniques [7, 20–22]. Typically, the inner loop controller (compensator) is designed by considering the converter dynamics and target system specifications and has the form of CRC and VRC. The CRC utilizes a current reference generated by voltage sensing information and thus makes the converter as a current source [18,22–29]. Commercial SAS systems mostly adopt this scheme. In contrast, the VRC uses voltage reference calculated from the output current sensing and thus behaves as a voltage source [30–33].

Meanwhile, according to the measurement variables, the control method can be further categorized as a voltage sensing (VS) [18,22–24,26,27,29], current sensing (CS) [30,32], and resistance sensing (RS) scheme [25,31,34]. Sometimes, real pilot PV modules are also used as PV characteristic generators [26]. A real PV panel is also used with artificial lighting in small-scale applications, but it does not support complex and accurate atmospheric pattern simulation. Such a system also has benefits such as 100% accurate PV behavior. However, a reference is generated according to a look-up table or PV characteristic equation to establish

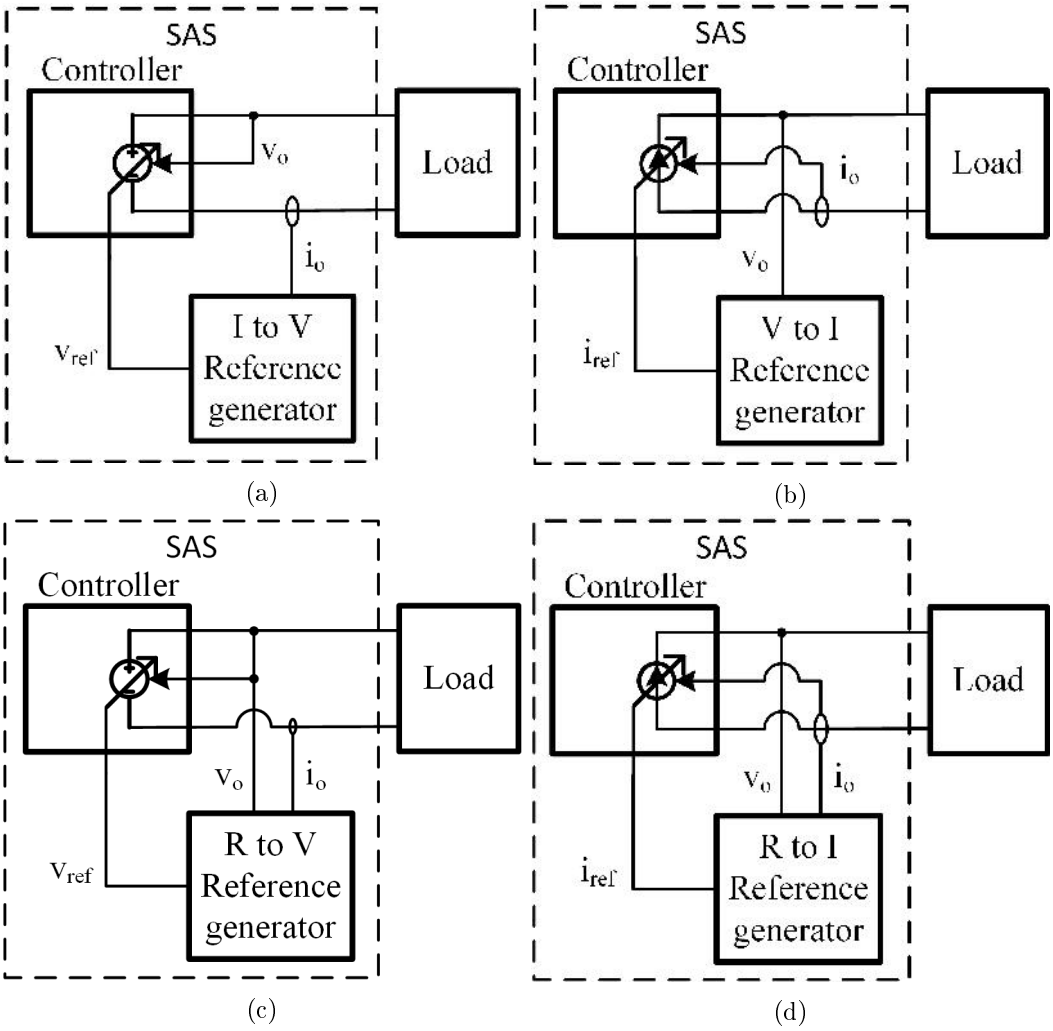


Figure 1-9: Block diagrams of SAS configuration (a) CS-VRC (b) VS-CRC (c) RS-VRC (d) RS-CRC.

Table 1.1: Previous works on SAS architecture

Ref.	Structure	Reference Generator	Controller
[23]	VS-CRC	PV equation	FS-MPC
[24]	VS-CRC	PV equation	PI
[26]	VS-CRC	Reference PV cell	PI
[22]	VS-CRC	Lookup table	PID
[27]	VS-CRC	Lookup table	PID
[18]	VS-CRC	Lookup table	Current mode PI
[29]	VS-CRC	Lookup table	PI
[25]	RS-CRC	PV equation	Current mode PI
[34]	RS-VRC	Lookup table	Boundary control law
[31]	RS-VRC	PV equation	Backstepping
[33]	CS-VRC	Lookup table	FLC
[30]	CS-VRC	Lookup table	Current mode PI
[32]	CS-VRC	PV equation	Type III
[28]	Hybrid (VS, RS-CRC)	Lookup table	PID
[35]	Hybrid (VS-CRC, CS-VRC)	Lookup table	PID
[6]	Hybrid (VS-CRC, CS-VRC,RS-VRC)	PV equation	PI

the operating point of the DC-DC converter. By combining VS, CS, and RS, a hybrid method is also possible [6,28,35], but it will not be taken into account in this study.

1.4 Problem Description and Objectives

In this section, four significant problems are identified in the SAS system. The SAS scheme highly demanded the stability of the SAS system, the operating range of the I-V curve, and control speed requirement.

In the case of stability, existing researchers were already conducted mainly about the interaction of SAS and different kinds of complex load such as constant power (CP) load, MPPT load, power curtailment load. However, some stability issues can be identified although with constant voltage, current, and resistance loads. They originated inside the SAS, and SAS internal stability analysis is rare in the literature. Especially, the stability of the SAS hardware inner loop is already taken into analysis, but the reference generator is considered an outside function of the SAS control loop.

1.4.1 Stability issue

Stability is one of the critical properties of SAS because SAS has to operate under various kinds of dynamics such as insolation, temperature, and load resistance. Thus, SAS has to endure a complicated dynamic scenario under a limited deviation of target operating conditions. Up to now, most of the existing SAS research has generally focused just on the steady-state accuracy of the simulator [6, 36]. Its stability is not intensively investigated, and only the stability of the primary control loop under constant reference signal is taken into account in most literature. For example, only a voltage controller is considered in VRC architecture, while the current controller is in CRC architecture. However, the reference signal also reflects the output changes and disturbs the entire SAS performance. Even though some papers mentioned the mechanism [6, 28, 35], these studies were limited to conceptual explanation and did not involve a systematic multi-loop analysis. The stability of the MPPT controller interface with PV module is widely discussed in [37,38], but it does not address the reference generator dynamic of the SAS. Thus, analysis and comparison of the performance of the SAS with different control architectures have not been tried.

As stated earlier, PV modules are non-linear devices with varying characteristics across their I-V curve. As shown in Fig. 1-5, the PV modules behave as a constant current source

(CSS) near the I_{sc} point, and the curve behaves as a constant voltage source near the V_{oc} point (VSS). Various mechanisms have been used in generating the reference control signal required for the control circuit. In the VRC system, the sensed current (CS) generates the reference signal, and it is shown to have a relatively stable output on the VSS but rather oscillatory in the CSS. The CSS has the slightest voltage variation for a significant divergence in current. An opposite trend is observed in the VSS, which has a significant voltage difference under the slightest current deviation results in the significant amplification in noise associated with CS. This results in an uneven system performance along the I-V characteristic curve of the PV module. Conversely, the CRC system whose reference signal is generated by sensing the voltage exhibits the exact opposite behavior of the VRC system. CS-VRC system shows stable and oscillatory outputs under VSS and CSS, respectively. Most commercial SAS is equipped with one of the above methods. To address the limitations in this method, many algorithms have been proposed different solutions. The resistance sensing (RS) SAS algorithms stand out and have been the next generation of the SAS algorithm. In this method, the sensed voltage to current ratio is used as the RS signal. Subsequently, R-V or R-I lookup table or modified PV equation (RS-VRC or RS-CRC) can be used for the reference generation.

VRC and CRC methods can extend the stable region along the PV I-V curve in the RS method. However, the resistance value is numerically closed to the infinity near the open circuit position, and reference generation fails to follow the PV characteristics. Nevertheless, the hybrid SAS system is also given an exciting solution. It uses both CS-VRC and VS-CRC methods in the relevant region, switching according to the operation point. It can cover the entire I-V curve but comparatively degraded the overall gain near the MPP, which is the most important for system testing. Further improvements in this algorithm involve incorporating RS-VRC or RS-CRC between VSS and CSS. Nonetheless, this results in mode changes between the regions and loses the smoothness of the I-V curve.

To analyze such behavior, dynamic responses to various inputs should be identified. Here, the temperature provides comparatively slow dynamics; thus, it was not much discussed in the literature. Studies about load dynamics were mostly discussed [18,32,39,40,40–42] and few studies can be found about the insolation dynamics [29,43,44]. Besides, small-signal modelings of SAS are carried out in [18,20,29,40–42,44] and that models were developed to address different configurations of the converter with the loads. Especially, [19,45–50] are discussed the interactions of PV characteristics with the MPPT loads and inner loop

dynamics.

However, it does not clearly address the stability issues in the dynamic range of the SAS and the effect of reference generator dynamics. According to the non-linear curvature of the I-V curve, the gradient is changed according to the operating point. Thus, the operating point affects the outer loop gain, which is caused to change the inner loop dynamics. In Chapter-2, this issue is deeply discussed [51–55] and explained by the small-signal model.

1.4.2 Operating range issue

Because of the non-linear gain discussed in Chapter-1.4.1, the current and voltage sensing method increase their feedback loop (outer loop) gain in the voltage and current source segment in the I-V curve, respectively. That effect limits the operating range of the I-V curve. However, when the stability of SAS improved, it positively affected the operating range.

Besides, the operating range of the SAS is discussed in a few studies [6, 7, 28, 35, 56–58]. The hybrid SAS concept is proposed as a solution to increase the operating range of the I-V curve. The study in [28] paper proposes a V-I and R-I hybrid lookup table method that overcomes the issues of the traditional single V-I lookup table method. However, the hybrid controllers of the SAS make other side-effects to the SAS operation, which is bounded with control region inter-changing. Those effects are discussed in Chapter-4.

The SAS operating range can be improved by using the RS method as an improvement of stability, but it also has an immense value near V_{oc} [37, 38] and hardware limitation for emulation of the open circuit operation and short circuit operation. The previous control speed improving studies such as [34], identify this issue but did not address it directly. Instead, the operating range is mentioned and considered as out scope of their topic.

However, operating range enhancement requires a hardware modification to have a significant improvement.

1.4.3 Fast reference generation

In the case of the SAS engine, the situation becomes a little bit more complex. It generates the target reference for the appropriate control action [26]. For example, when the operating point is on the left side of the maximum power point, the desired current reference, I_{ref}, needs to be calculated from the PV model equation by the sensed terminal voltage, V_{sense}, of the PV panel, and then the control loop is regulating the output current of the DC/DC

converter to keep up with the PV panel characteristic. When on the right side of the maximum power point, the reference voltage, V_{ref}, would be calculated from the sensed current, I_{sense}, to control the output voltage of SAS. In the hardware implementation, choosing the correct algorithm to solve the model equation is critical in emulating the PV characteristics.

As the problems in the conventional algorithms, the PV model equation shown in (1.6) is highly non-linear, inherently implicit, and has no analytical solution. The current appears on both sides of the equation, and the separation of variables is not easy because of the exponential term. That means either calculating the current from a given voltage or the voltage from a given current is not a simple task. Conventionally, iterative root-finding algorithms are used to find its numerical solution. For example, with a given sensed PV terminal voltage, V_{sense}, and the initial guess of the current value, I_0, the next guess of the current, I_1, is calculated successively. After sufficient iteration steps, we can find a final solution that meets the termination criteria of the numerical calculation. On the opposite side of the maximum power point, a similar mechanism works with the role of the current, and voltage is reversed.

Among various numerical algorithms, the simplest one is to use the simple fixed-point iteration method [59] with linear convergence given by

$$I_n = g(V_{sense}, I_{n-1}), n = 1, 2, 3, ... \tag{1.10}$$

where n is the iteration number. More frequently, a faster algorithm with quadratic convergence is Newton-Raphson method [60] using the iteration equation of

$$I_n = I_{n-1} - \frac{f(V_{sense}, I_{n-1})}{f'(V_{sense}, I_{n-1})}, n = 1, 2, 3, ... \tag{1.11}$$

where the prime denotes the differentiation with respect to the terminal current. Other higher-order algorithms like Halley's method [61] is similar to Newton's method and, when it works correctly, it has cubic convergence. However, the higher the order of the algorithm is, the less stable it is and the more computationally expensive it gets. For these reasons, higher-order methods are typically not used. However, in conventional algorithms, a need for such iteration steps degrades the performance of PV emulation. This problem becomes a more serious effect, especially in microcontroller-based SAS systems, because it usually has limited computing power and memory resources. For these reasons, a non-iterative

alternative should be investigated.

Faster control speed is a general requirement for most kinds of converters. In the case of SAS, it needs to satisfy the requirements of the dynamic characteristics in EN50530 PV PSC standard test procedure [10]. According to that, SAS should be minimally supported to absorb a ripple twice the line frequency (120Hz), but the operating performance depends on the device under test.

The MPPT algorithm such as incremental conductance (INC), perturb and observation P&O, hill climbing (HC) always try to increase the tracking speed to maximize the MPPT efficiency [10]. For example, the newly proposed r-INC [62, 63] has a control bandwidth 10kHz. According to the Nyquist sampling theorem, switching frequency (f_{sw}) must be two times higher than the controller bandwidth [13], but practically, it should be larger by four-times [12]. [11] used this frequency ratio five times. So the SAS controller bandwidth should be at least five times higher.

The control speed requirement is essential in the Global MPPT (GMPPT) algorithm. When a shadow partially covers the PV array, the monotonic shape of the I-V curve is changed into a segment. GMPPT has a sub-algorithm named "Global Peak Search (GPS)" to detect the maximum power peak from among available peaks. Different kinds of GPS are proposed in literature [64–72] and all of them have a typical behavior that operating point is switched fast to have the samples to predict the GMPP.

For example, the newly proposed adaptive partial shading determinant algorithm can be considered [3, 73]. The algorithm is shown in Fig. 1-10. When the GPS is triggered, the operating point is forcefully moved into desired positions according to the GPS algorithm for an instant. Then instant time should be as much as a minimum because the extractable power is not maximum within this instant. Hopefully, GPS will provide the desired reference directly, and the outer loop is skipped. However, the SAS inner loop should be faster enough to generate the operating point for this application. Thus, a faster but sufficiently accurate SAS method is highly motivated.

In the case of the SAS engine, the situation becomes a little bit more complex. It generates the target reference for the appropriate control action [26]. For example, when the operating point is on the left side of the maximum power point, the desired current reference, I_{ref}, needs to be calculated from the PV model equation by the sensed terminal voltage, V_{sense}, of the PV panel, and then the control loop is regulating the output current of the DC/DC converter to keep up with the PV panel characteristic. When on the right

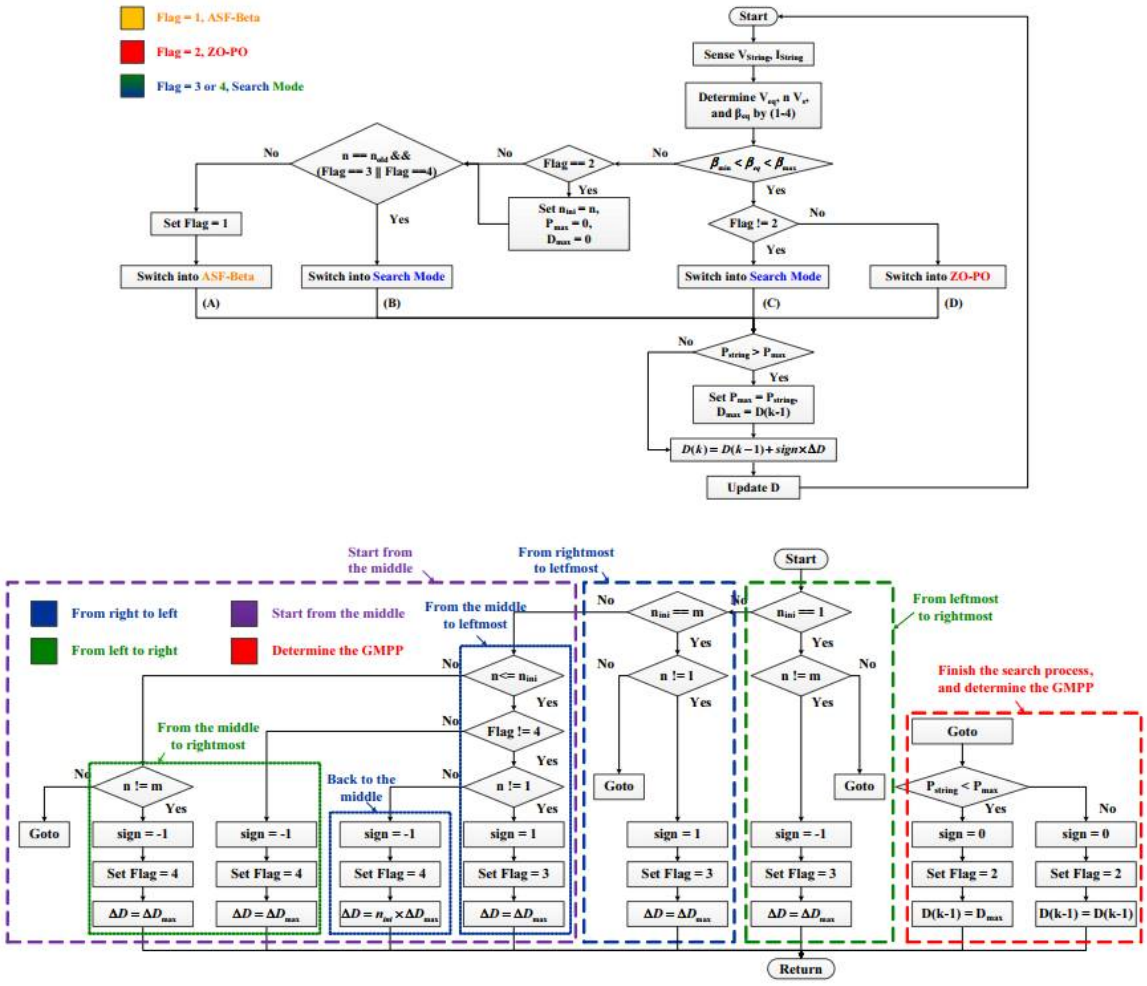


Figure 1-10: Flowcharts of Global MPPT algorithms [3]

side of the maximum power point, the reference voltage, V_{ref}, would be calculated from the sensed current, I_{sense}, to control the output voltage of SAS. Choosing the correct algorithm to solve the model equation is critical in emulating the PV characteristics in both software and hardware implementation cases.

As the problems in the conventional algorithms, the PV model equation shown in 1.6 is highly non-linear, inherently implicit, and has no analytical solution. The current show on both sides of the equation and variable separation is not easy because of the exponential term. That means calculating the current from a given voltage or the voltage from a given current is not a simple task. Conventionally, iterative root-finding algorithms are used to find its numerical solution. For example, with a given sensed PV terminal voltage, V_{sense}, and the initial guess of the current value, I_0, the next guess of the current, I_1, is calculated successively. After sufficient iteration steps, we can find a final solution that meets the termination criteria of the numerical calculation. On the opposite side of the maximum power point, a similar mechanism works with the role of the current, and voltage is reversed.

1.5 Contributions and Thesis Organization

In this study, all the fundamental components of the SAS systems are introduced within the scope of stability. The PV characteristics and existing algorithms are analyzed and illustrated; this includes the current, voltage, and resistance sensing method and their impact on stability. This study proposes five promising techniques for the improvement of the SAS scheme. A new small-signal analyzing method is proposed in the beginning and used for the evaluation of other improved systems. Due to the implicitness of available PV mode, a super elliptical curve is adopted as the PV curve. Then it is used to verify the proposed unified PV controller, which enhances the SAS analytical simplicity and speed of the SAS reference generator. Besides, the explicit Lambert-Ω approximate PV model is also proposed as a fast convergence reference generator. Finally, the SAS hardware is improved by introducing the bidirectional converter.

- In Chapter-2, the adoption of the super elliptical model and the small-signal model is demonstrated. As the sensing method, VS, CS, and RS systems are modeled. Significantly, the insolation and temperature effect is considered a disturbance to the closed-loop, and a model is developed according to that. Then the stability of SAS with different load types is modeled. Constant voltage (CV), constant current (CC),

and constant resistance (CR) with MPPT loads are included in the small-signal model.

- The stability analysis is done in the Chapter-3. The main for SAS architectures such as CS-VRC, VS-CRC, RS-VRC, and RS-CRC are analyzed and explained the behavior in terms of stability. The time delay of the reference generator modifies the gain and phase margin of the overall loop, and it is described in a bode plot. Then, different load types such as CV, CC, and CR are examined and distinguished from the stable and unstable configurations. Accordingly, frequency domain and time domain simulation are proceeded and verified by the hardware test.

- Two innovated controller strategies are demonstrated in Chapter-4. The unified controller is introduced here, and the proposed small-signal model to analyze the stability. Its performance is compared with the conventional hybrid controller. Besides, the approximated Lambert-Ω method is proposed to activate the fast convergence speed of the SAS reference generator with minimal error. First, the explicit form is derived and checked the accuracy. Then, the required program cycle time for different sensing voltages is compared. On the other hand, the super-ellipse approximation is used for the analysis as well as the SAS reference generator. The curve fitting is proceeded by finding the order of super-ellipse. Then, its accuracy is compared with the datasheet values and conventional single-diode model. Finally, the synchronous buck topology is adopted to enhance the speed performance of hardware. Its slew rate is compared with a conventional buck converter for verification.

Chapter 2

Modeling of SAS system

2.1 Overview

In this chapter, SAS elements are modeled individually. The typical SAS system is shown in Fig. 2-1. At first, the reference generator is modeled in section 2.2. According to the PV model equation, SAS should control the voltage or current to hold the operating point according to the given load. Thus, the SAS converter needs a reference that is decided according to the PV characteristic. This reference is calculated by sensing output voltage and current in the outer loop. Insolation and temperature also affected the reference, so it is also considered. According to the (1.6) I_{pv} appears in both side of the equation; thus, it cannot solve in one step and need a numerical solving method to use it. Due to the explicitness of the PV characteristic equation, a customized super-elliptic equation is used for the analysis and discusses the compatibility to avoid the complexity of explicitness.

Second, the power stage mode is discussed in section 2.3. The unterminated model

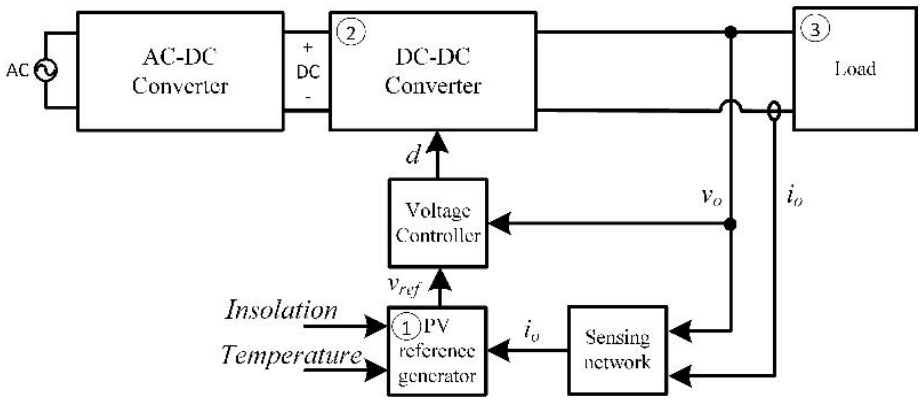


Figure 2-1: Typical SAS system

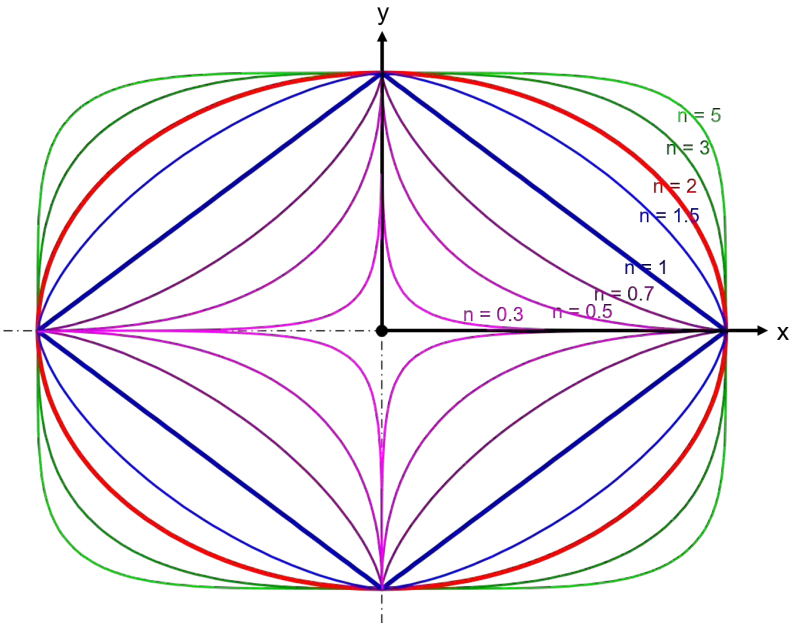


Figure 2-2: Typical super elliptical curve [4]

is used as a voltage controller and current controller, then simplified to the general buck converter transfer functions.

Third, the load system for SAS mode is discussed in section 2.4. The CV, CC, and CR loads are modeled with SAS, and loop modification is discussed. The MPPT loads are considered as resistive loads.

2.2 Modeling of reference generator

2.2.1 Elliptical approximation

As mentioned in Chapter-1, the sensed voltage value produces the current reference, or the sensed current value produces the voltage reference. The I-V characteristic of the PV curve is an exponential function where the current and voltage are defined implicitly; it is not easy to be analytically solved in a closed form, which means its stability analysis becomes rather complicated. Thus, this study introduces a super elliptic curve (Lamé curve) as an approximated PV curve to simplify the small-signal modeling by resolving the implicitness and focusing more on stability analysis.Typical super elliptic curve function is shown in Fig. 2-2 [4]. To emulate the I-V curve, the general super elliptic equation

$$\left|\frac{x}{a}\right|^n + \left|\frac{y}{b}\right|^n = 1 \tag{2.1}$$

can be adopted and used as the approximated PV curve.

$$\left[\frac{v}{V_{oc}}\right]^n + \left[\frac{i}{I_{sc}}\right]^n = 1 \tag{2.2}$$

It is needed to obtain the relevant super elliptic curve which goes through $(V_{oc}, 0)$,$(0, I_{sc})$, and (V_{mpp}, I_{mpp}) points. Thus, the "n" can be calculated by solving the logarithmic equation

$$\left[\frac{V_{mpp}}{V_{oc}}\right]^n + \left[\frac{I_{mpp}}{I_{sc}}\right]^n = 1 \tag{2.3}$$

$$\left[\frac{V_{mpp}}{V_{oc}}\right] = A, \left[\frac{I_{mpp}}{I_{sc}}\right] = B \tag{2.4}$$

To solve this equation, let's take

$$n_{i+1} = \frac{-B^{n_i}}{\log\left(\frac{A}{B}\right)}; \tag{2.5}$$

This equation can be simply solved by iteration of (2.5) [74]. Now, let us consider that after obtaining the n_i up to one decimal point, it can be taken as "n" of the relevant super-ellipse. The first quadrant of the super elliptical curves in Fig. 2-3 has a similar shape as the PV curve in the I-V plane but can be described by a simple explicit function. Since the tangential slope of the elliptical curve at two ends, i.e., the open-circuit voltage point $(V_{oc}, 0)$ and the short-circuit current point $(0, I_{sc})$, approaches infinity and zero respectively, and thus varies more widely compared to the original PV curve, all tangent slopes within the PV module can be dealt with by the approximated curve.

At this time, it is easy to see that the differentiation of the power obtains the maximum power point of the proposed elliptical equation, and the voltage and current of the maximum power point of the PV module (MSX120) are observed as follows, respectively.

$$V_{mpp} = 36.6V, I_{mpp} = 3.35A \tag{2.6}$$

Therefore, considering the fill factor,

$$FF = \frac{V_{mpp} I_{mpp}}{V_{oc} I_{sc}}, \tag{2.7}$$

the elliptical curve has an FF of 0.75. Since the fill factor of datasheet value is typically

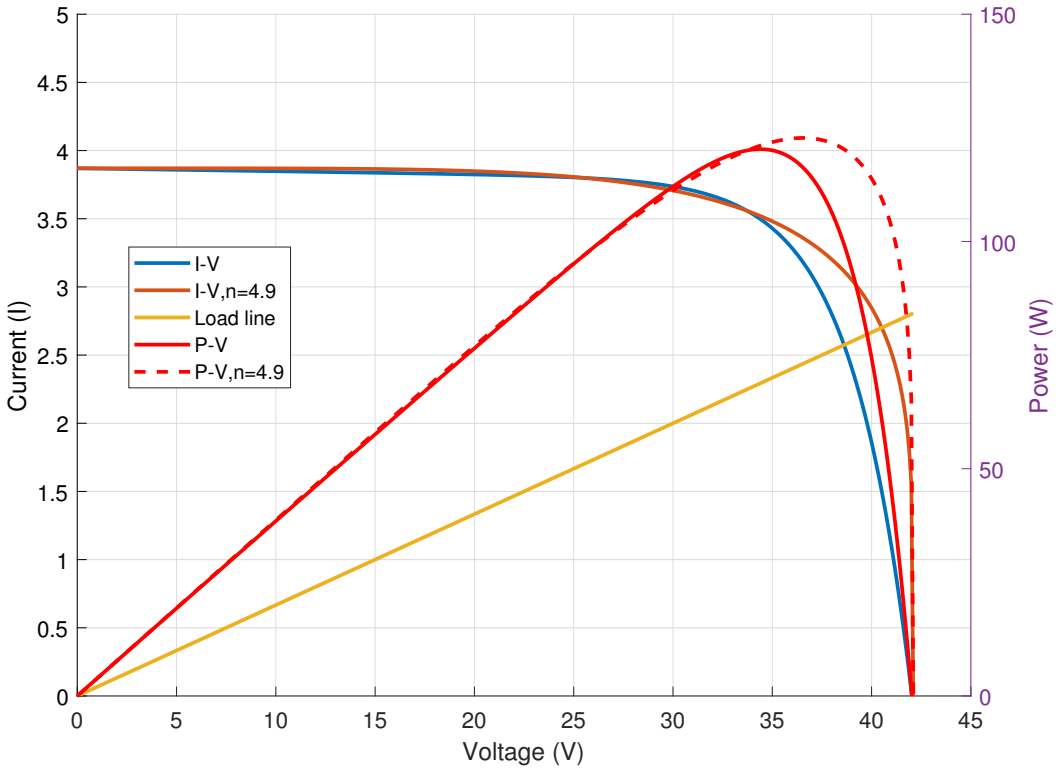


Figure 2-3: I-V and P-V characteristic of ellipse approximation MSX120

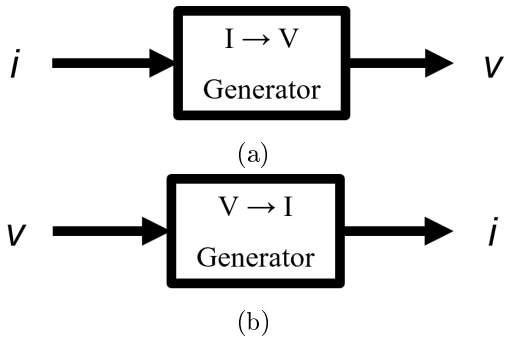


Figure 2-4: Large signal block diagram of reference generator (a) CS-VRC (b) VS-CRC

calculated as

$$FF_{MSX120} = \frac{33.7 \times 3.56}{42.1 \times 3.87} = 0.74. \tag{2.8}$$

2.2.2 Small-signal modeling of reference generator

2.2.2.1 CS reference system

In the CS-VRC structure, the large signal model of the voltage reference is shown in Fig. 2-4a and can be generated by

$$v_{ref} = V_{oc}\sqrt[n]{1-(\frac{i}{I_{sc}})^n} \tag{2.9}$$

and n-2 case becomes

$$v_{ref} = V_{oc}\sqrt{1-(\frac{i}{I_{sc}})} \tag{2.10}$$

where i is the measured current of SAS. The small-signal gain which is evaluated at the point of operation (Vop, Iop) is the sensed current signal with respect to the voltage reference obtained by differentiation (2.9) and is evaluated at the point of operation (V_{op}, I_{op}) as a trans-resistance.

$$k_{v_{ref},i} = \frac{\hat{v_{ref}}}{\hat{i}}\Big|_{(V_{op},I_{op})} = -\frac{V_{oc}I_{op}^{(n-1)}}{I_{sc}^n}\left[1-\left(\frac{I_{op}}{I_{sc}}\right)^n\right]^{(\frac{1}{n}-1)} \tag{2.11}$$

when the n=2,

$$k_{v_{ref},i} = \frac{\hat{v_{ref}}}{\hat{i}}\Big|_{(V_{op},I_{op})} = -\frac{V_{oc}}{I_{sc}^2}\frac{I_{op}}{\sqrt{1-\left(\frac{I_{op}}{I_{sc}}\right)^2}} \tag{2.12}$$

2.2.2.2 VS reference system

In the VS-CRC structure, the large signal model of the voltage reference is shown in Fig. 2-4b and can be generated by

$$i_{ref} = I_{sc}\sqrt[n]{1-(\frac{v}{V_{oc}})^n} \tag{2.13}$$

and n-2 case becomes

$$i_{ref} = I_{sc}\sqrt{1-(\frac{v}{V_{oc}})^2} \tag{2.14}$$

where v is the measured output voltage of SAS.

The small-signal gain from the sensed voltage signal to the current reference value at the operating point (V_{op}, I_{op}) will appear in the form of trans-conductance. For the general case,

$$k_{i_{ref},v} = \frac{\hat{i_{ref}}}{\hat{v}}\Big|_{(V_{op},I_{op})} = -\frac{I_{sc}V_{op}^{(n-1)}}{V_{oc}^n}\left[1-\left(\frac{V_{op}}{V_{oc}}\right)^n\right]^{(\frac{1}{n}-1)}. \tag{2.15}$$

when the n=2,

$$k_{i_{ref},v} = \frac{\hat{i_{ref}}}{\hat{v}}\Big|_{(V_{op},I_{op})} = -\frac{I_{sc}}{V_{oc}^2}\frac{V_{op}}{\sqrt{1-\left(\frac{V_{op}}{V_{oc}}\right)^2}} \tag{2.16}$$

2.2.2.3 RS reference system

RS reference system shows a considerable improvement of the SAS system. Although it senses the same operating point as CS and VS system, it can provide a more stable response because voltage or current is highly affected by controller dynamics and noise, but load resistance is almost constant under such a condition. However, it needs a theoretical analysis to prove this statement.

In the case of RS reference generators, the modeling process becomes a little more complicated. The reference generation consists of two steps as the resistance information is obtained by measuring both the output voltage and current as shown in Fig. 2-5a. First, it calculates the instantaneous resistance through the output voltage and current by 2.17; next, it generates the corresponding voltage or current reference value from the v to i ratio.

$$r = \frac{v}{i}. \tag{2.17}$$

To obtain the reference, (2.17) is substituted into (2.9) or (2.13). Then, the large-signal model of the RS-VRC is shown in Fig. 2-5b and the signal becomes

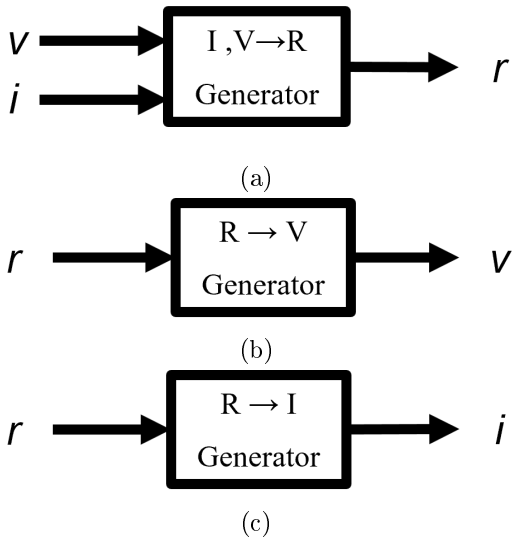


Figure 2-5: Large-signal block diagram of RS system (a) Resistance sensing (b) RS-VRC (c) RS-CRC

$$v_{ref,RS} = \frac{1}{\sqrt[n]{\left(\frac{1}{rI_{sc}}\right)^n + \left(\frac{1}{V_{oc}}\right)^n}}. \tag{2.18}$$

For the n=2 case

$$v_{ref,RS} = \frac{1}{\sqrt{\left(\frac{1}{rI_{sc}}\right)^2 + \left(\frac{1}{V_{oc}}\right)^2}} \tag{2.19}$$

Similarly, the large-signal model of the RS-CRC is shown in Fig. 2-5c and the signal becomes

$$i_{ref,RS} = \frac{1}{\sqrt[n]{\left(\frac{r}{V_{oc}}\right)^n + \left(\frac{1}{I_{sc}}\right)^n}}. \tag{2.20}$$

and the reference signal in RS-CRC becomes

$$i_{ref,RS} = \frac{1}{\sqrt{\left(\frac{r}{V_{oc}}\right)^2 + \left(\frac{1}{I_{sc}}\right)^2}}. \tag{2.21}$$

Here, r is the resistance calculated by sensed output voltage and current in (2.17).

According to (2.17), the small-signal model is shown in Fig. 2-6 and describing the first step is given by

$$\hat{r} = k_{rv}\hat{v} + k_{ri}\hat{i} \tag{2.22}$$

where the two small-signal gains at the operating point are given as differential gains re-

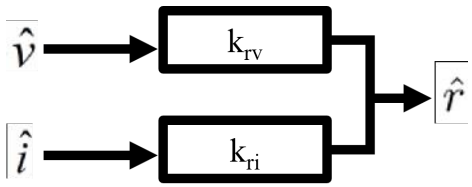


Figure 2-6: Small-signal block diagram of RS system

spectively, as shown below,

$$k_{rv} = \frac{\hat{r}}{\hat{v}}\Big|_{(V_{op},I_{op})} = \frac{1}{I_{op}}, k_{ri} = \frac{\hat{r}}{\hat{i}}\Big|_{(V_{op},I_{op})} = -\frac{V_{op}}{I_{op}^2} \tag{2.23}$$

In addition, the small-signal model describing the second step is given in two cases. If a reference is given by $v_{ref} = f(r)$ as in (2.18), the small-signal gain at the operating point (V_{op}, I_{op}) is given as follows:

$$k_{v_{ref},r} = \frac{\hat{v_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = \frac{1}{r^{1+n} I_{sc}^n \left(\left(\frac{1}{rI_{sc}}\right)^n + \left(\frac{1}{V_{oc}}\right)^n\right)^{\frac{1}{n}+1}} \tag{2.24}$$

Similarly, when the reference is in the form of $i_{ref} = g(r)$ as in (2.20), the small-signal gain is given by

$$k_{i_{ref},r} = \frac{\hat{i_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = -\frac{r^{n+1}}{V_{oc}^n \left(\left(\frac{r}{V_{oc}}\right)^n + \left(\frac{1}{I_{sc}}\right)^n\right)^{\frac{1}{n}+1}}. \tag{2.25}$$

For the n=2 case

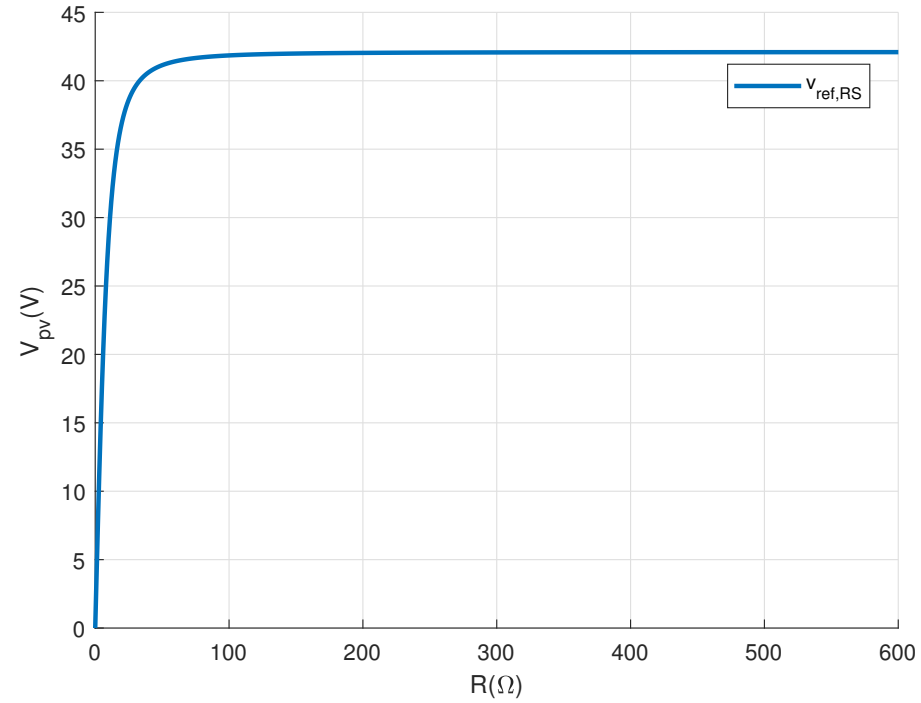
$$k_{v_{ref},r} = \frac{\hat{v_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = \frac{1}{r^3 I_{sc}^2 \left(\left(\frac{1}{rI_{sc}}\right)^2 + \left(\frac{1}{V_{oc}}\right)^2\right)^{\frac{3}{2}}} \tag{2.26}$$

and

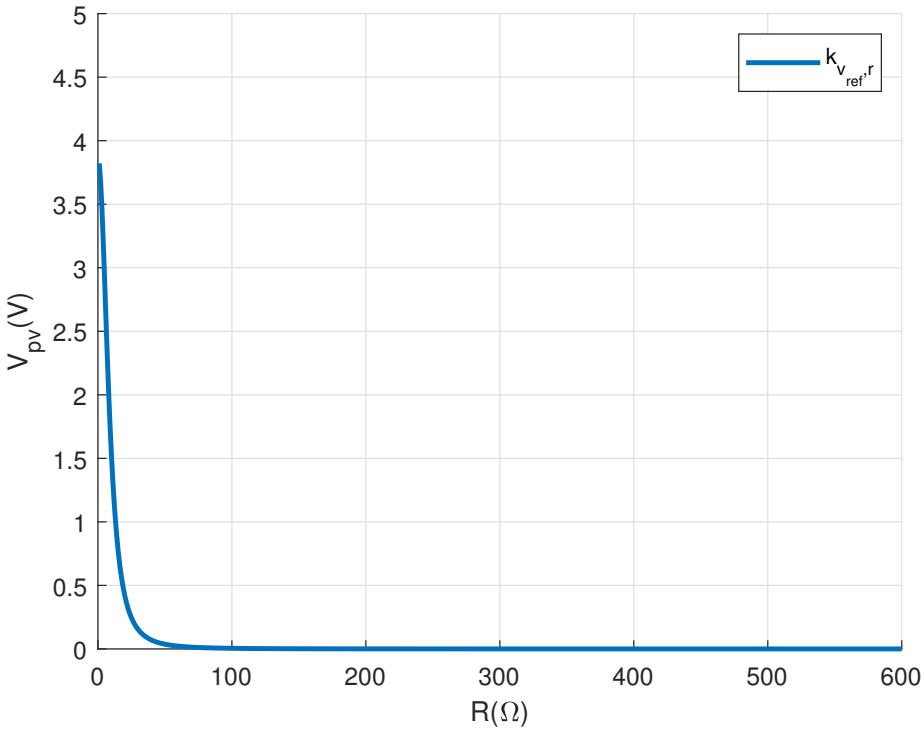
$$k_{i_{ref},r} = \frac{\hat{i_{ref}}}{\hat{r}}\Big|_{(V_{op},I_{op})} = -\frac{r}{V_{oc}^2 \left(\left(\frac{r}{V_{oc}}\right)^2 + \left(\frac{1}{I_{sc}}\right)^2\right)^{\frac{3}{2}}}. \tag{2.27}$$

The $v_{ref,RS}$ and $k_{v_{ref},r}$ trend can be understand as shown in Figs. 2-7.

It is possible to use this function to analyze the model, but the n=2 curve is used further in this study. In most cases, the reference generation usually accompanies the computation time and purposely adds a delay because the reference signal should not be faster than the primary control loop. Thus, a time delay function, L(s), must be added to model the



(a)



(b)

Figure 2-7: RS-VRC reference generator (a) RS characteristic curve (b) RS generator gain

reference generation, which can be simplified by the Padé approximation [75].

$$L(s) = e^{-st_d} \approx \frac{1-\alpha s}{1+\alpha s}; \alpha = t_d/2 \tag{2.28}$$

where the t_d accounts for such a time delay effect in the reference generation.

2.2.2.4 Insolation and temperature effect on reference system

Insolation and temperature always affect the SAS reference generator. In the commercial SAS, the insolation and temperature pattern generator have complex pre-defined pattern storage and time-varying simulation task. In addition, SAS manufacturers always try to provide a user-friendly interface to compose patterns. That makes the insolation and temperature modeling demanded highly, but very few research was done before.

To develop the small-signal model for this case, it is needed to consider the relation of the SAS model with the insolation and temperature. For the super elliptical model, the V_{oc},I_{sc}, and MPP points should be obtained from the insolation and temperature relation. Such a study can be found in [76] and target equation as noted below.

$$I_{sc} = I_{sc,STC}\frac{\phi}{\phi,STC}\left[1 + k_i(\theta - \theta_{STC})\right] \tag{2.29}$$

$$V_{oc} = V_{oc,STC} + NA_{STC}\frac{k\theta}{q}ln\left(\frac{\phi}{\phi_{STC}}\right) + k_v(\theta - \theta_{STC}) \tag{2.30}$$

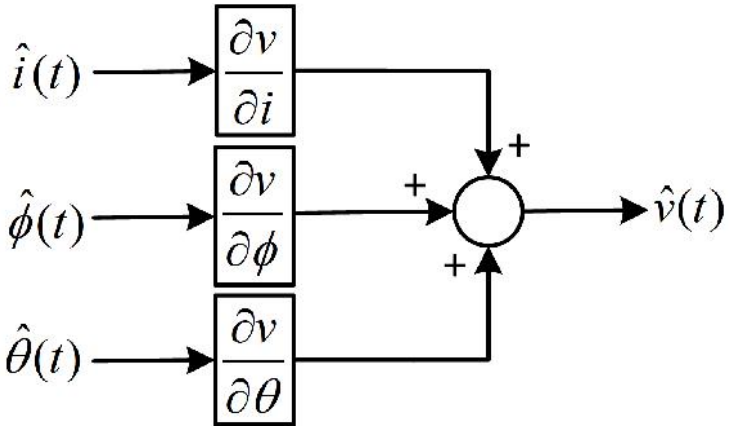
$$I_{mpp} = I_{mpp,STC}\frac{\phi}{\phi_{STC}}\left[1 + k_{i,mpp}(\theta - \theta_{STC})\right] \tag{2.31}$$

$$V_{mpp} = V_{mpp,STC} + NA_{STC}\frac{k\theta}{q}ln\left(\frac{\phi}{\phi_{STC}}\right) + k_v, mpp(\theta - \theta_{STC}) \tag{2.32}$$

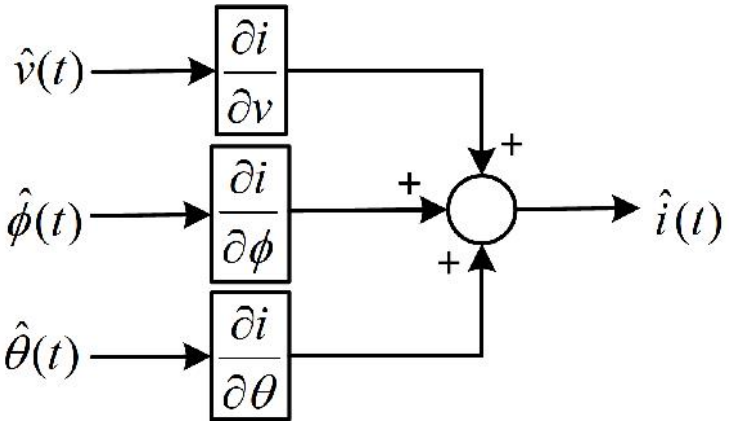
where ϕ and θ are irradiance and temperature, and the quantity with subscript STC denotes its value under STC. In the above equations, every quantity except A_{STC}, and $k_{i,mpp}$, and $k_{v,mpp}$ is usually specified in the manufacturer's datasheet. The diode ideality factor evaluated under STC, A_{STC}, is determined in the initialization routine and was discussed in [76]. The other two unknown constants, $k_{i,mpp}$, and $k_{v,mpp}$ are the temperature coefficients of MPP variation. Though they are not usually found in datasheet, approximation can be used instead of real value.

$$k_{i,mpp} \cong k_i, k_{v,mpp} \cong k_v \tag{2.33}$$

In [77], such an approximation has been successfully used to estimate the temperature



(a)



(b)

Figure 2-8: Small signal block diagram for insolation and temperature (a) Voltage reference generator (b) Current reference generator

dependency of MPP and, it is reported that the error in the output current caused by this approximation is trivial. Moreover, the error in the voltage, even if it is slightly large, is less than 5% [78]. Therefore, it is reasonable to use the k_i and k_v instead of $k_{i,mpp}$ and $k_{v,mpp}$ to express the thermal drift of the datasheet parameters.

The small-signal model for the insolation and temperature can be introduced as shown in Fig. 2-8. They affect to the outer loop as a disturbance. Here, the small-signal model has two cases for voltage and current reference system. If a reference is given by $v_{ref} = f(i, \phi, \theta)$, the small-signal gain at the operating point (V_{mpp}, I_{mpp}) is given as follows:

$$k_{v_{ref},\phi} = \frac{\hat{v_{ref}}}{\hat{\phi}}\Big|_{(V_{mpp},I_{mpp},V_{oc},I_{oc})} \tag{2.34}$$

and

$$k_{v_{ref},\theta} = \frac{\hat{v_{ref}}}{\hat{\theta}}\Big|_{(V_{mpp},I_{mpp},V_{oc},I_{oc})} \tag{2.35}$$

Similarly, when the reference is in the form of $i_{ref} = g(v, \phi, \theta)$, the small-signal gain is given by

$$k_{i_{ref},\phi} = \frac{\hat{i_{ref}}}{\hat{\phi}}\Big|_{(V_{mpp},I_{mpp},V_{oc},I_{oc})} \tag{2.36}$$

and

$$k_{i_{ref},\theta} = \frac{\hat{i_{ref}}}{\hat{\theta}}\Big|_{(V_{mpp},I_{mpp},V_{oc},I_{oc})} \tag{2.37}$$

2.3 Modeling of power stage

2.3.1 Current-terminated buck converter model

By decoupling the converter dynamics and load dynamics, it is easily possible to change the type of the load. To adapt the unterminated converter model, let us model the converter as shown in Fig. 2-9a. It is a two port network and has three input ($\hat{v_s}, \hat{i_o}$, and $\hat{d}$) and two output ($\hat{v_o}, \hat{i_s}$). By replacing the load with a current source as shown in Fig. 2-9b. Then the small-signal block diagram can be modified with considering the output impedance, Z_p as shown in Fig. 2-9c.

The differential output voltage can be defined accordingly.

$$\hat{v_o} = dv_o(\hat{v_s}, \hat{i_o}, \hat{d}) \tag{2.38}$$

Thus,

$$\hat{v_o} \cong \frac{\hat{v_o}}{\hat{v_s}}\Big|_{(\hat{i_o},\hat{d})=0}\hat{v_s} - \frac{\hat{v_o}}{\hat{i_s}}\Big|_{(\hat{v_s},\hat{d})=0}\hat{i_s} + \frac{\hat{v_o}}{\hat{d}}\Big|_{(\hat{i_o},\hat{v_s})=0}\hat{d} \tag{2.39}$$

Here, $\hat{v_s}$ is not interested because a well-regulated power supply provides the input voltage of the buck converter; thus, $\hat{v_s}$ is taken as zero. Then the unterminated model equations of voltage source converter can be derived as

$$G_{vd,u}(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)}\Big|_{(\hat{i_o},\hat{d})=0} = V_s\frac{1 + sCr_c}{1 + sCr_c + s^2LC} \tag{2.40}$$

and

$$Z_p, u(s) = \frac{\hat{v_o}(s)}{\hat{i_o}(s)}\Big|_{(\hat{i_o},\hat{v_s})=0} = \frac{sL}{1 + sCr_c + s^2LC}. \tag{2.41}$$

2.3.2 Voltage-terminated buck converter model

Similarly, the unterminated model equations of current source converter diagrams are shown in Fig. 2-10, and model equations can be derived as

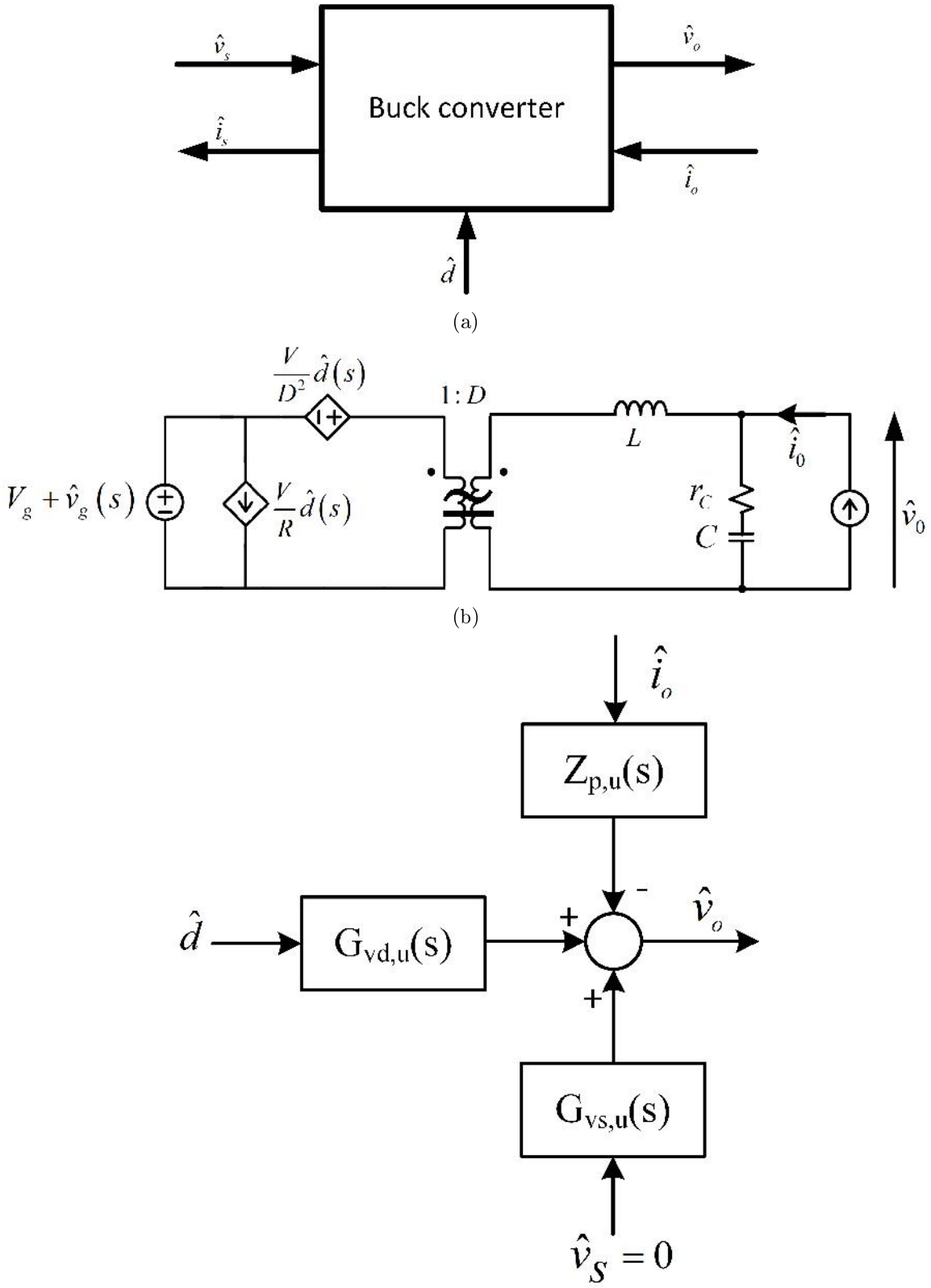


Figure 2-9: Current-terminated converter model (a) Block diagram (b) Equivalent circuit (c) Small-signal model

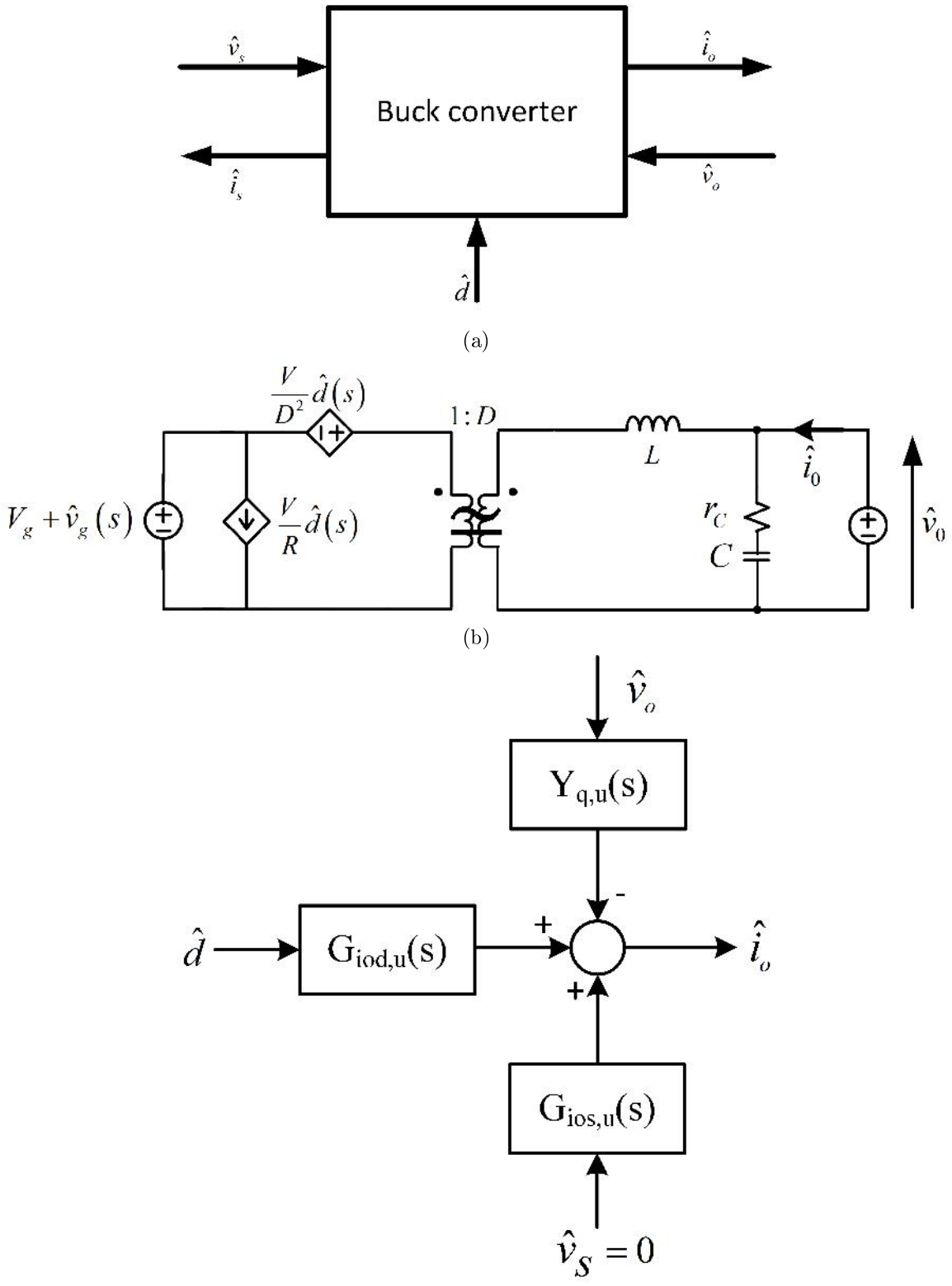


Figure 2-10: Voltage-terminated converter model (a) Block diagram (b) Equivalent circuit (c) Small-signal model

$$G_{i_o d,u}(s) = \frac{\hat{i_o}(s)}{\hat{d}(s)} = \frac{V_s}{sL} \tag{2.42}$$

and

$$Y_{q,u}(s) = \frac{\hat{i_o}(s)}{\hat{v_o}(s)} = -\frac{1 + sCr_c + s^2LC}{sL + s^2LCr_c}. \tag{2.43}$$

2.3.3 Resistive load-terminated buck converter model

The resistive load-terminated model diagrams of buck converter are shown in Fig. 2-11. Its two transfer functions, G_{vd} and $G_{i_o d}$ are derived by unterminated model in (2.44) and (2.45) [79].

$$G_{vd}(s) = G_{vd,u}(s)\frac{1}{1 + \frac{Z_{p,u}(s)}{R_L}} \tag{2.44}$$

and

$$G_{i_o d}(s) = G_{i_o d,u}(s)\frac{1}{1 + R_L Y_{q,u}(s)} \tag{2.45}$$

Resistance terminated model equations can be derived by substituting (2.40) and (2.41), and obtain the 2.46.

$$G_{vd}(s) = \frac{\hat{v_o}(s)}{\hat{d}(s)} = V_s\frac{(1 + sCr_c)}{1 + (Cr_c + \frac{L}{R_L})s + LC(1 + \frac{r_c}{R_L})s^2} \tag{2.46}$$

Similarly, (2.47) resistance terminated current model equations can be derived by substituting 2.42 and 2.43, and obtain the 2.47.

$$G_{i_o d}(s) = \frac{\hat{i_o}(s)}{\hat{d}(s)} = \frac{V_s}{R_L}\frac{(1 + sCr_c)}{1 + (Cr_c + \frac{L}{R_L})s + LC(1 + \frac{r_c}{R_L})s^2} \tag{2.47}$$

2.4 Load side modeling

The small-signal model of the SAS can be further discussed with different kinds of loads. The behavior of the load modifies the small-signal model, so a possible load combination should be considered. Thus, this modeling is needed to configure the optimal controller structure of the system by representing the relationship between the control method of the PCS and SAS. In this section, three types of SAS loads are modeled.

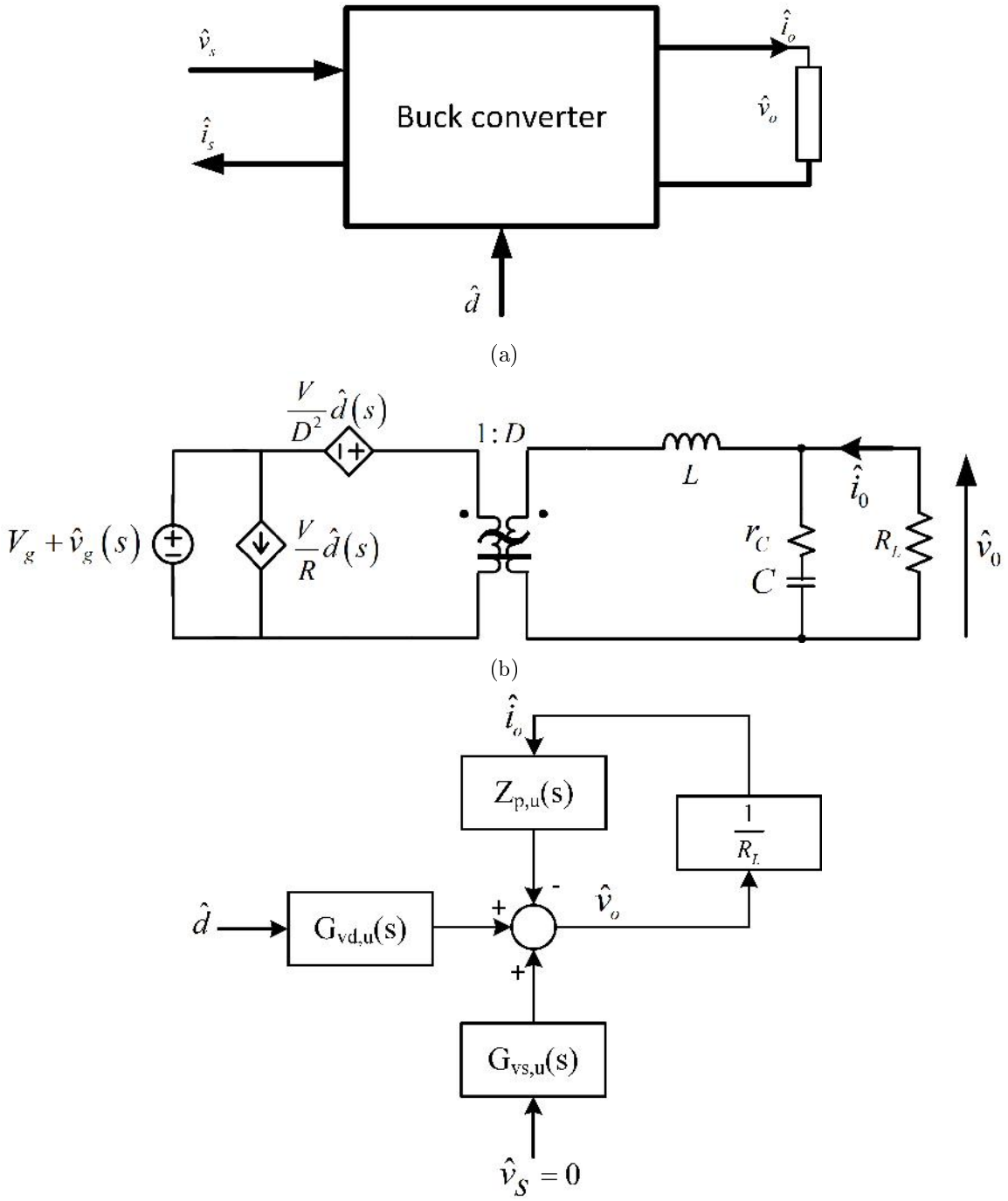
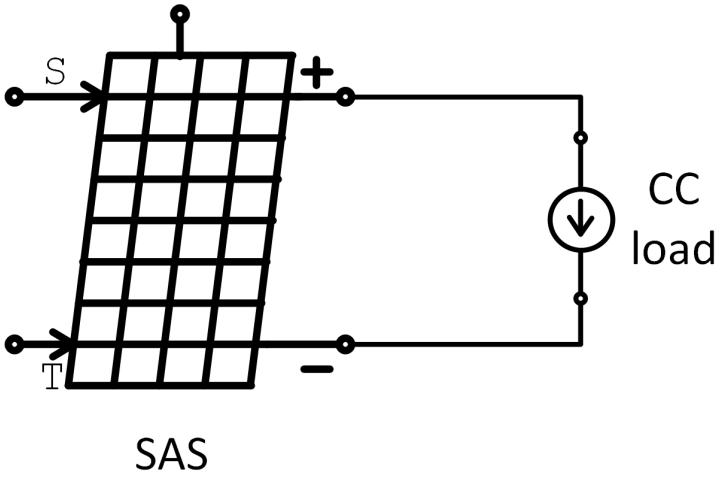
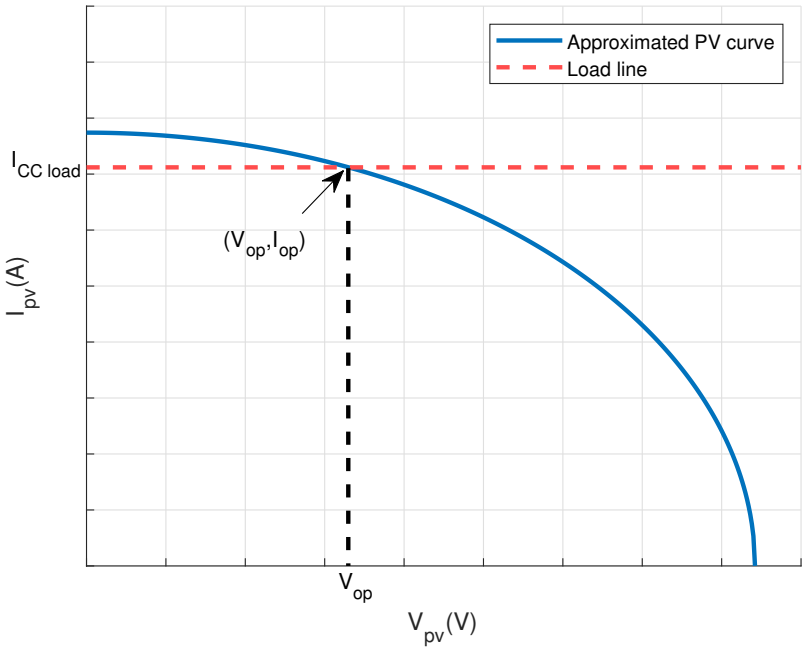


Figure 2-11: Resistive load-terminated converter model (a) Block diagram (b) Equivalent circuit (c) Small-signal model



(a)



(b)

Figure 2-12: Unterminated current converter model (a) System block diagram (b) CC load line with approximated PV curve

2.4.1 Constant current (CC) load

Even constant current (CC) loads are rare in the PV system; it is sometimes observed in PCS operated by fractional short circuit current (FSCC) MPPT algorithm [80]. When the PCS is controlled by an average current mode controller or charge current mode controller, it is affected to SAS as a CC load. The CC load line can be plotted with a PV characteristic curve as shown in Fig. 2-12.

2.4.2 Constant voltage (CV) load

Constant voltage (CV) loads can be found in many applications, including battery and super-capacitor energy storage systems. Another example is the PCS operated by fractional open circuit voltage MPPT algorithms (FOCV) [81]. In this case, the CV load holds a constant voltage, and the PV curve determines its current. CV load line can be plotted with PV characteristic curve as shown in Fig. 2-13. To keep the positive current flow from the PV module, the voltage of the CV load should be less than the V_{oc}. According to the PV equation (1.6), V_{oc} is slightly varying according to the insolation. As a result, CV load voltage should be set in the vicinity of $V_{mpp,STC}$ to extract the maximum power.

2.4.3 Constant resistance (CR) load

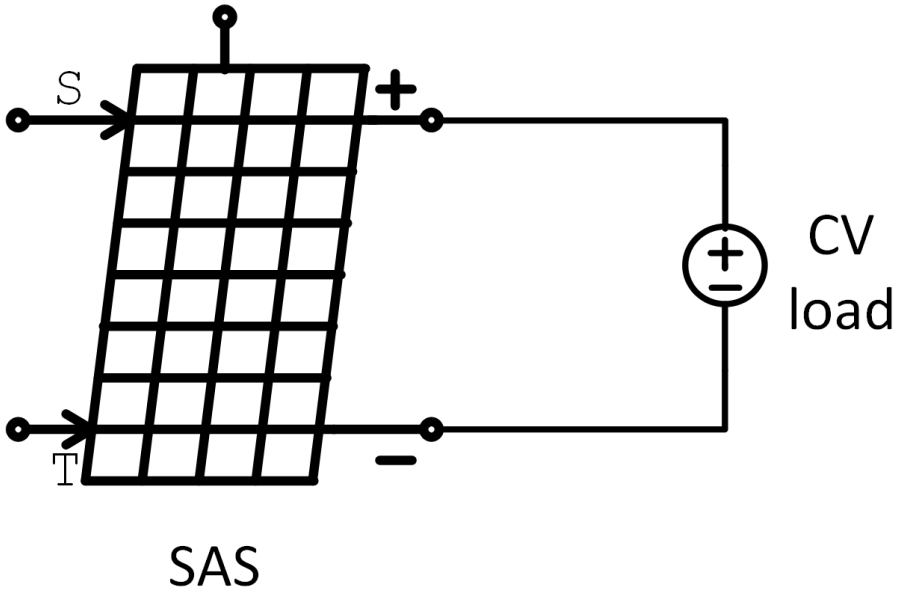
CR load line can be plotted with PV characteristic curve as shown in Fig. 2-14. The most common load of the PV array is the resistance load. Because PCS operating with Hill climbing (HC), perturb, and observation ($P\&O$), incremental conductance (INC) algorithms can be regarded as resistive loads. This section shows that MPPT operations can be described as a simple way, which tracks the voltage derivation of PV power until it becomes zero.

$$\frac{dp}{dv} = 0 \tag{2.48}$$

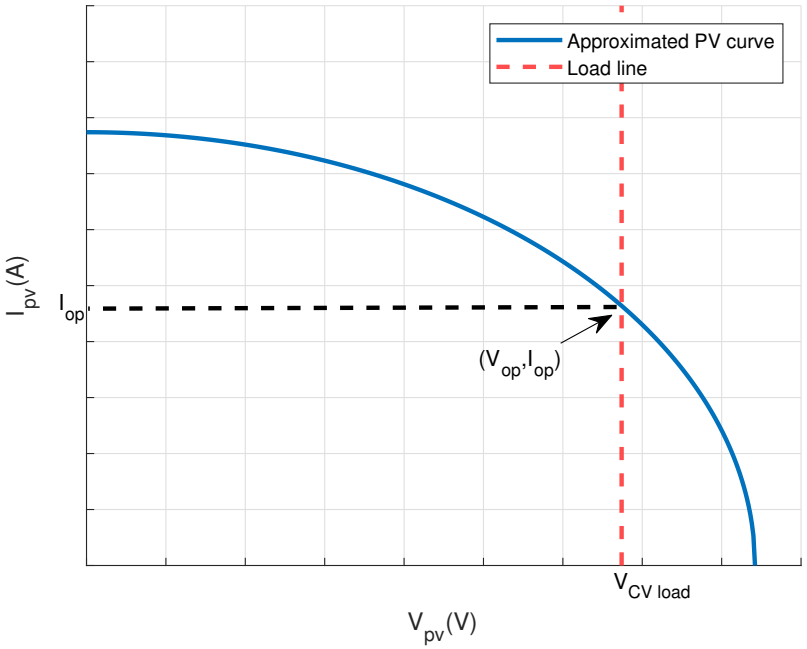
On the other hand, MPPT also adjusts the average load resistance (input resistance of MPPT PCS), which always intersects the MPP of the I-V curve.

In addition, the control architecture of MPPT can interact with the SAS controller in two ways. To minimize the interaction, the gain cross-over frequency of the MPPT controller should be much lower than (at least five times lower; according to the Nyquist theorem [11, 13]) the SAS gain cross-over frequency. This phenomenon and input dynamics of the MPPT controller are studied in many scopes. In [82], resistive control MPPT converter is proposed as a battery charger. Here, the current loop conflict is solved by introducing the resistive-controlled architecture. A large-signal stability of solar PCS is deeply discussed in [83–86]. Mostly, constant power loads have stable and unstable points, and their dynamics were illustrated. However, as a conclusion of that study, the above controller can be considered a resistive controller and used in MPPT PCS. Thus, it can be regarded that the MPPT controllers are a kind of variable resistive loads.

It is needed to consider the compatibility of SAS with grid-connected PV systems. Gen-

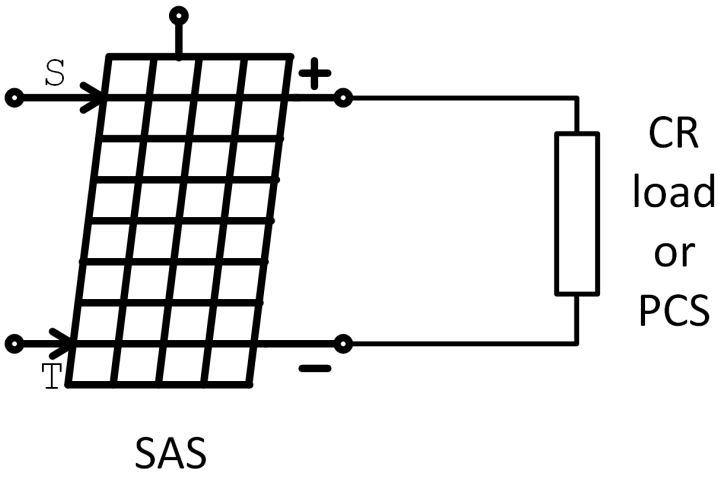


(a)

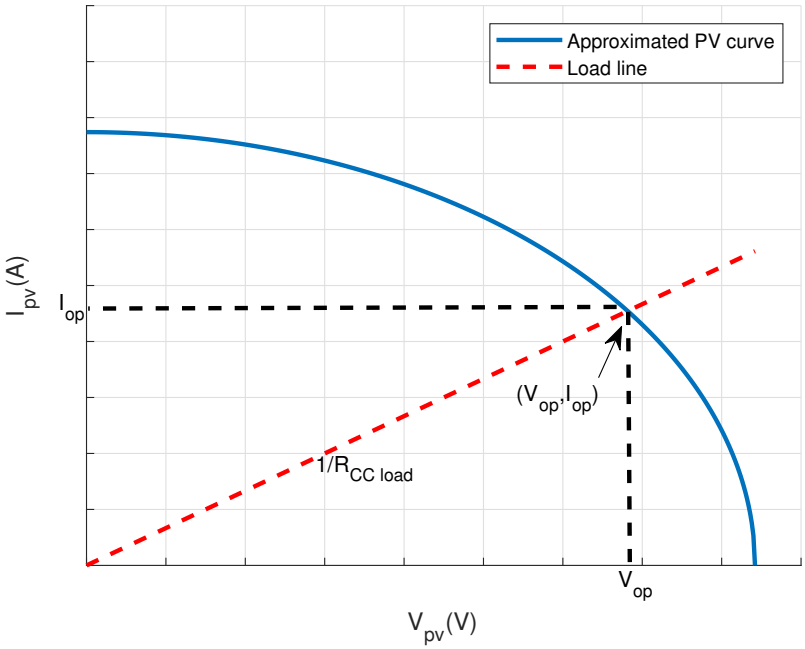


(b)

Figure 2-13: Unterminated voltage converter model (a) System block diagram (b) CV load line with approximated PV curve



(a)



(b)

Figure 2-14: Unterminated voltage converter model (a) System block diagram (b) CR load line with approximated PV curve

erally, the MPPT controller continuously tracks the MPP regardless of the network power demand. Because solar power is a free source, thus continuous MPPT is commercially important. A few applications can be found in which PV system is used as a dynamic power source for regulating the demand fluctuation [87]. However, MPPT does not directly transform the grid-related dynamics into the PV array side; thus, the MPPT resistive model is still valid in the grid-connected MPPT system.

2.5 Conclusion

In this chapter, the super-elliptical approximation model is introduced and demonstrated. The order of super-ellipse is changed according to the PV model parameter, insolation, and temperature. This order "n" is a logarithmic function; thus, a simple iteration method is used to obtain it. Then, the small-signal model is derived for four SAS systems. The delay of the reference generator is considered and modeled by using the Padé approximation. Especially, insolation and temperature are also included in the model as a disturbance for the main control loop. The power stage is modeled using the unterminated model and proves the equality with the general transfer function. Finally, stability with three kinds of load, CV, CC, and CR, are modeled. Here, the MPPT loads are considered as a variable resistive load according to the literature review.

Chapter 3

Stability Analysis of SAS system

3.1 Overview

In this section, the primary four types of SAS controllers are analyzed using the developed small-signal model. Then the stability with CV, CC, and CR loads are analyzed. To verify the proposed model, the system is implemented on simulation and hardware. First, the power plant is designed according to the target specification. It is used to verify the system by frequency-domain and time-domain simulation. Then, the hardware is implemented for further confirmation of the proposed model.

3.2 Small-signal analysis of SAS with CR load

3.2.1 CS-VRC configuration

The overall small-signal block diagram of the CS-VRC structure is shown in Fig. 3-1a and large signal model is shown in Fig. 3-1b. Because the main control loop is composed of a voltage controller, it appears to be a single loop system, but the voltage reference is also time-varying by measuring the output current, so another external loop exists. As a result, a double-loop system must be considered in which the reference generation forms the outer loop, and the voltage loop forms the inner loop. The voltage and the reference loop gains in the CS-VRC structure are defined by (3.1) and (3.2), respectively:

$$T_v(s) = F_m C(s) G_{vd}(s) \tag{3.1}$$

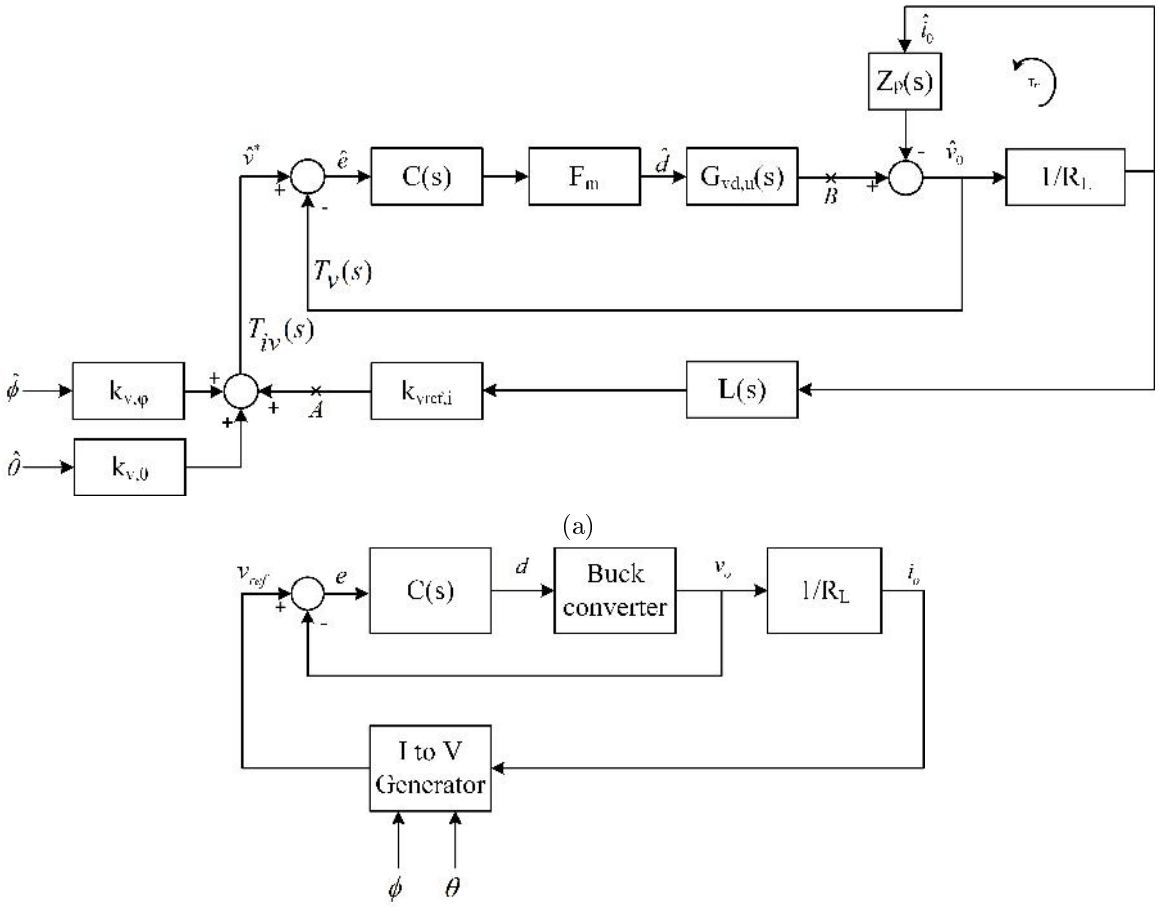


Figure 3-1: Modeling of CS-VRC (a) Small-signal block diagram (b) Large-signal block diagram

and

$$T_{iv}(s) = F_m C(s) G_{vd}(s) \frac{k_{v_{ref},i} L(s)}{R_L} \tag{3.2}$$

where $k_{v_{ref},i}$ is the gain defined in (2.16), and L(s) represents the time delay function in (2.28).

When interpreting these multi-loop systems, the literature [88] has mentioned a problem in which the loop gains T(s) are not defined uniformly but rather are dependent on the location of the signal injection point or loop-breaking point [79]. If the loop is interpreted at point A in Fig. 3-1a, the outer loop gain is obtained by

$$T_A(s) = \frac{T_{iv}(s)}{1 + T_v(s)}. \tag{3.3}$$

If the loop is interpreted at point B in Fig. 3-1a, the overall loop gain is obtained as

$$T_B(s) = T_v(s) + T_{iv}(s). \tag{3.4}$$

The individual loop gain can be interpreted to see the stability and response characteristics of the whole system. This paper utilizes the overall loop gain $T_B(s)$ to check the loop interactions.

By substituting (3.2) and (3.3) into (3.4), we obtain

$$T_B(s) = F_m C(s) G_{vd}(s) K_1(s) \tag{3.5}$$

where $K_1(s)$ can be defined as

$$K_1(s) = (1 - k_1 L(s)); k_1 = \frac{k_{v_{ref},i}}{R_L} \tag{3.6}$$

describing the interference from the outer loop. If $K_1(s)$ is unity, no loop interaction exists between the outer and inner loop gains. Hence, the system behaves like a single loop control system. From the above equation, it can be deduced that $K_1(s)$ is dependent on the resistance ratio, k_1, and the time delay effect, L(s).

The resistance ratio factor, k_1 denotes the ratio of incremental resistance of the PV curve to the load resistance. By definition, it is clear that k_1 always has a negative value, showing the following trends:

$$(V_{op}, I_{op}) \rightarrow (V_{oc}, 0) : k_1 \rightarrow 0\,(< 0)$$
$$(V_{op}, I_{op}) \rightarrow (V_{mpp}, I_{mpp}) : k_1 \rightarrow -1$$
$$(V_{op}, I_{op}) \rightarrow (0, I_{sc}) : k_1 \rightarrow -\infty$$

This means that k_1 becomes a minimal negative value when the operating point is near the open-circuit condition or the voltage source region, while k_1 becomes an immense negative value when the operating point is near the short circuit condition or current source region.

The second factor L(s), describes the time delay effect in the reference generation process. It is mainly caused by a low sampling frequency setting in the outer loop. Because the reference generation process requires slower operation than the inner loop controller, it contains the intentional time delay in the outer loop path.

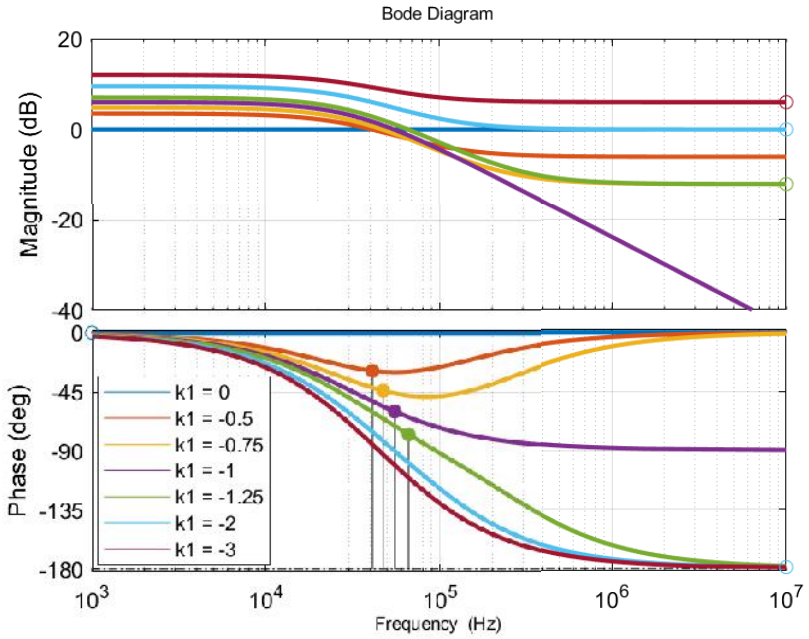
To investigate the loop interactions according to the operating point variations and the time delay setting, $K_1(s)$ is rearranged with Padé approximation in (3.7) and then becomes

$$K_1(s) = (1 - k_1)\frac{1 + \frac{\alpha(1+k_1)s}{(1-k_1)}}{1 + \alpha s}. \tag{3.7}$$

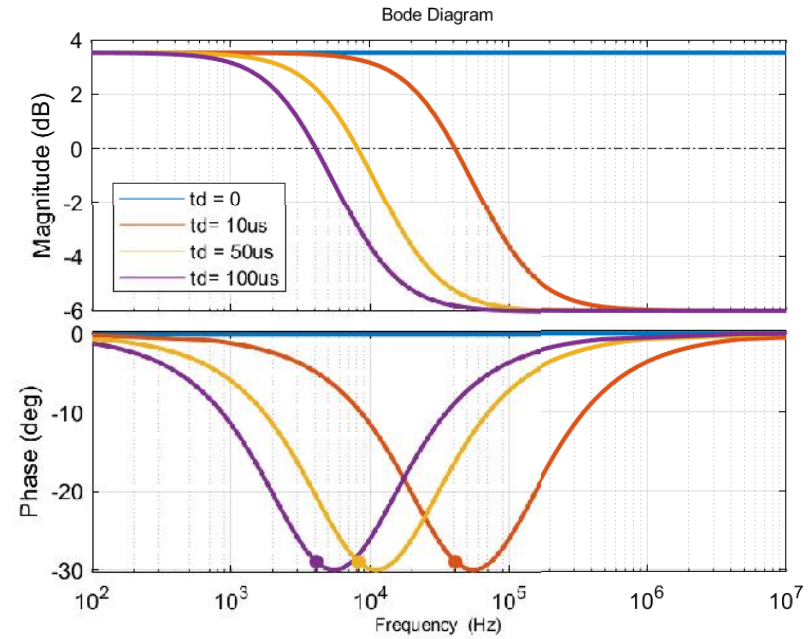
The Bode plot of $K_1(s)$ in Fig. 3-2 explains the influence of various operating conditions and delay time in the reference generation. Fig. 3-2a shows the frequency response of $K_1(s)$ according to k_1 variations when the time delay, t_d is assumed to be 10μs. It can be observed that when $-1 < k_1 < 0$ where the SAS operates in the voltage source region, $K_1(s)$ contains a left-half-plane zero resulting in a small phase delay angle, so there is not much loop interaction. The zero disappears when $k = -1$, where the SAS operates at MPPT. On the contrary, when $k_1 < -1$ where the SAS operates in the current source region, $K_1(s)$ has a right-half-plane zero causing additional phase delay, severely degrading the system stability. Fig. 3-2b shows $K_1(s)$ according to t_d variations when $k_1 = -0.5$. This shows that the stability could have further deteriorated if more delay is assigned to the reference generation process even without the operating point change.

3.2.2 VS-CRC configuration

Figure 3-3a shows the VS-CRC structure where the main control loop is composed of a current loop, and the sensed voltage generates the reference current and large signal model



(a)



(b)

Figure 3-2: Loop interaction function $K_1(s)$ (a) according to k_1 when t_d=10μs (b) according to t_d when k=-0.5

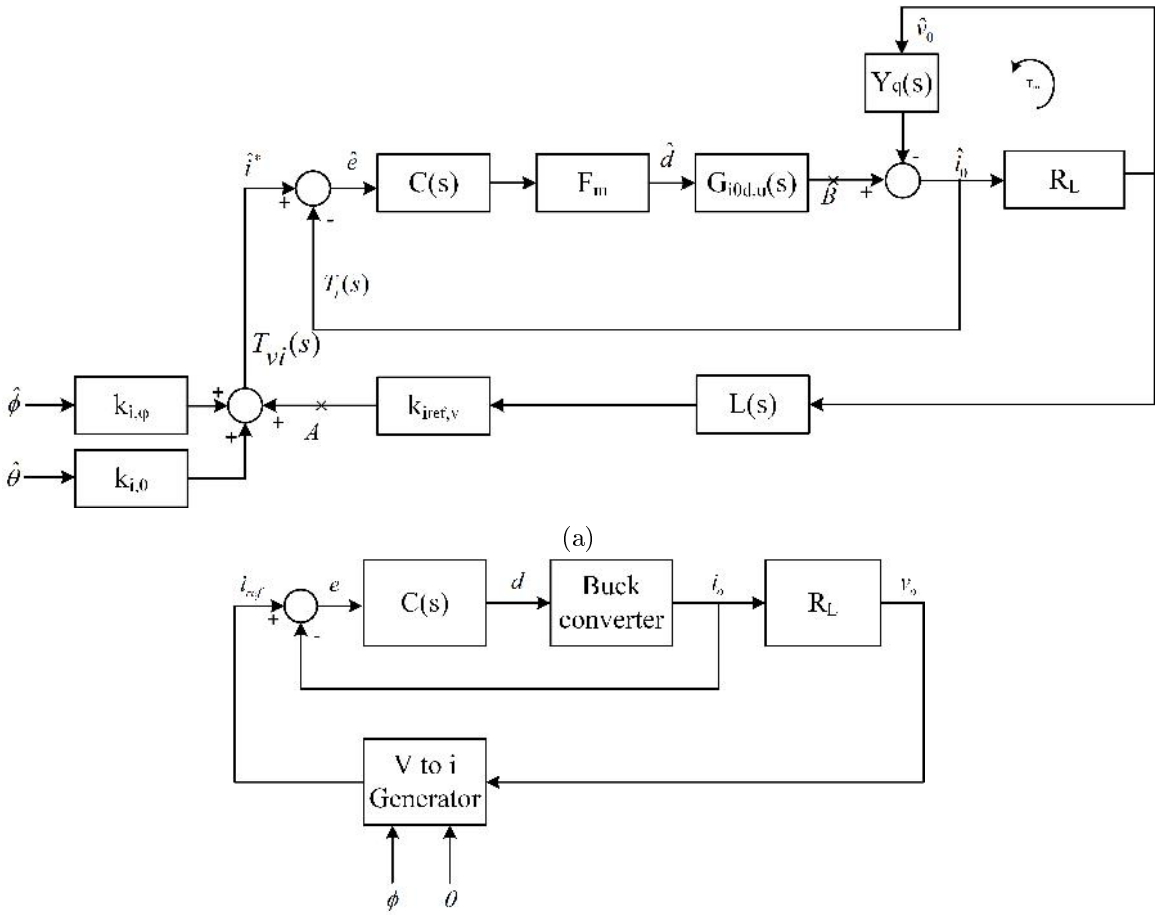


Figure 3-3: Modeling of VS-CRC (a) Small-signal block diagram (b) Large-signal block diagram

is shown in Fig. 3-1b. Then, the loop gain at the breaking point B can be written as

$$T_B(s) = T_i(s) + T_{vi}(s) \tag{3.8}$$

where the loop gains of the VS-CRC structure can be written as

$$T_i(s) = F_m C(s) G_{i_o d}(s) \tag{3.9}$$

and

$$T_{vi}(s) = F_m C(s) G_{i_o d}(s) R_L k_{i_{ref},v} L(s) \tag{3.10}$$

Accordingly, the overall loop gain become

$$T_B(s) = F_m C(s) G_{i_o d}(s) K_2(s) \tag{3.11}$$

where, $K_2(s)$ is defined by (3.12) to describe the extent to which the reference loop causes interference with the inner loop.

$$K_2(s) = 1 - k_2 L(s); k_2 = k_{i_{ref},v} R_L \tag{3.12}$$

Unlike the CS-VRC system, the resistance ratio (k_2) is proportional to the load resistance (R_L). Moreover, it has the following trends:

$$\begin{aligned}
&(V_{op}, I_{op}) \rightarrow (V_{oc}, 0) : k_2 \rightarrow -\infty \\
&(V_{op}, I_{op}) \rightarrow (V_{mpp}, I_{mpp}) : k_2 \rightarrow -1 \\
&(V_{op}, I_{op}) \rightarrow (0, I_{sc}) : k_2 \rightarrow 0\,(< 0)
\end{aligned}$$

It should be noted that $K_2(s)$ has a similar tendency to $K_1(s)$ but has opposite operating point characteristics and has the form of (3.13) by Padé approximation.

$$K_2(s) = (1 - k_2) \frac{1 + \frac{\alpha(1+k_2)s}{(1-k_2)}}{1 + \alpha s} \tag{3.13}$$

This reflects that the VS-CRC system is not affected by loop interactions near the current source segment, but it will have a low phase margin in the voltage source segment.

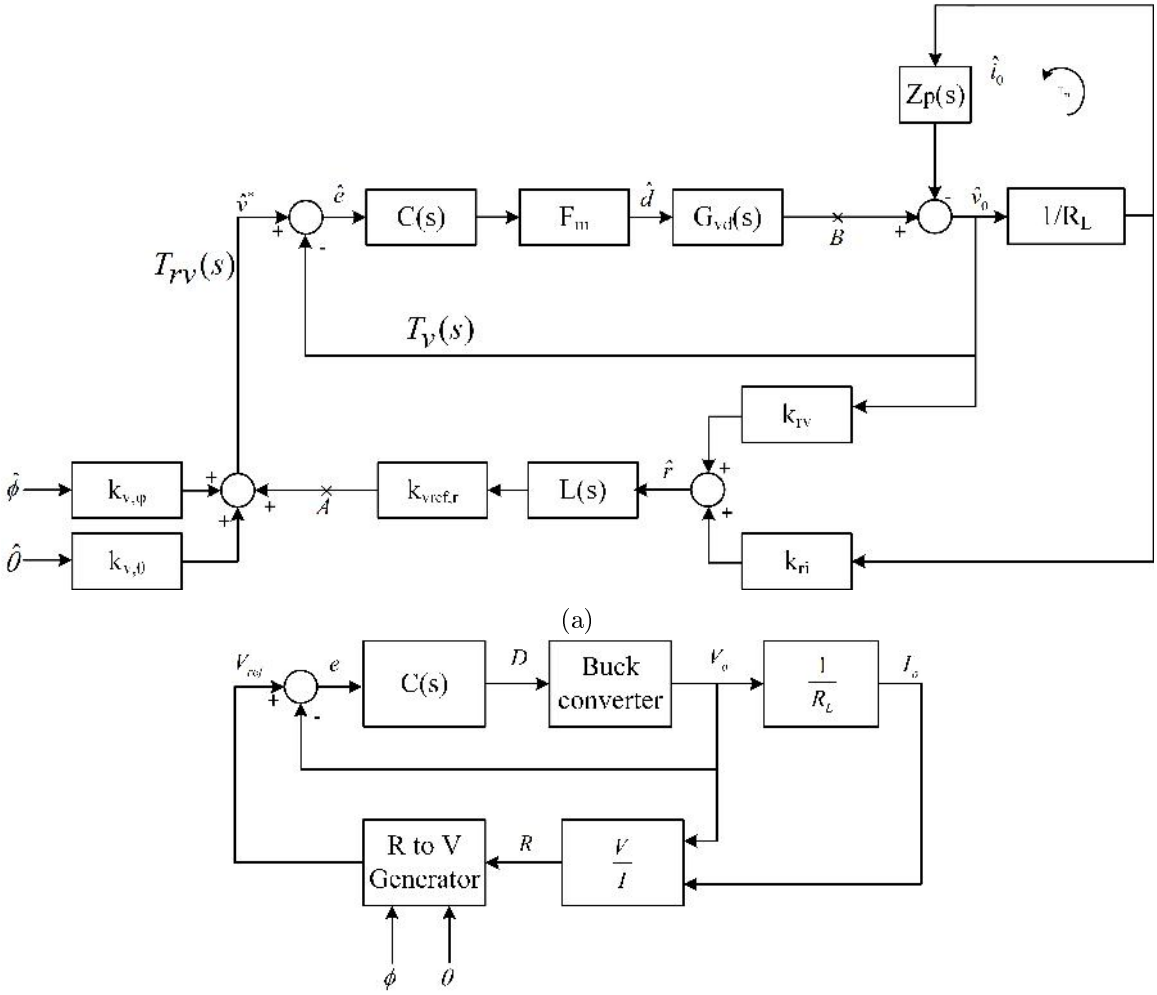


Figure 3-4: Modeling of RS-VRC (a) Small-signal block diagram (b) Large-signal block diagram

3.2.3 RS-VRC configuration

Meanwhile, the RS-VRC configuration can be modeled as shown in Fig. 3-4a, and current loop gain and reference loop gain are given as follows, respectively. and large signal model is shown in Fig. 3-1b.

$$T_v(s) = F_m C(s) G_{vd}(s) \tag{3.14}$$

and

$$T_{rv}(s) = F_m C(s) G_{vd}(s) k_{v_{ref},r} \left(k_{rv} + \frac{k_{ri}}{R_L} \right) L(s) \tag{3.15}$$

Thus, the overall loop gain becomes

$$T_B(s) = F_m C(s) G_{vd}(s) K_3(s) \tag{3.16}$$

where

$$K_3(s) = 1 - k_{v_{ref},r}\left(k_{rv} + \frac{k_{ri}}{R_L}\right)L(s) \tag{3.17}$$

and $k_{v_{ref},r}$ is the small-signal gain according to the curve slope of the solar module.

Since the following condition is always met:

$$k_{rv} + \frac{k_{ri}}{R_L} = \frac{1}{I_{op}} - \frac{V_{op}/I_{op}^2}{V_{op}/I_{op}} = 0, \tag{3.18}$$

by substituting (2.23) into (3.17), we get $K_3(s) \equiv 1$. This observation shows how the structure of resistance sensing reference generation can eliminate the effects of inter-loop interactions regardless of the operating point variations and the delay of the reference-point generation, which is beneficial in view of the system stability.

3.2.4 RS-CRC configuration

The RS-CRC configuration in Fig. 3-5a is dual to RS-VRC and large signal model is shown in Fig. 3-1b.The current loop gain and reference loop gain of the RS-CRC structure can be written as

$$T_i(s) = F_m C(s) G_{i_o d}(s) \tag{3.19}$$

and

$$T_{ri}(s) = F_m C(s) G_{i_o d}(s) L(s) k_{i_{ref},r}\left(k_{ri} + k_{rv} R_L\right) \tag{3.20}$$

Accordingly, the overall loop gain becomes

$$T_B(s) = F_m C(s) G_{i_o d}(s) K_4(s) \tag{3.21}$$

where

$$K_4(s) = 1 - k_{i_{ref},r}\left(k_{ri} + k_{rv} R_L\right) L(s). \tag{3.22}$$

Similarly, to the RS-VRC system, $K_4(s)$ is unity since

$$k_{ri} + k_{rv} R_L = -\frac{i_o}{V_o} + \frac{1}{I_{op}}\frac{V_{op}}{I_{op}} = 0. \tag{3.23}$$

This result again confirms the ability of the RS system to eliminate the operating point influence on the loop interaction.

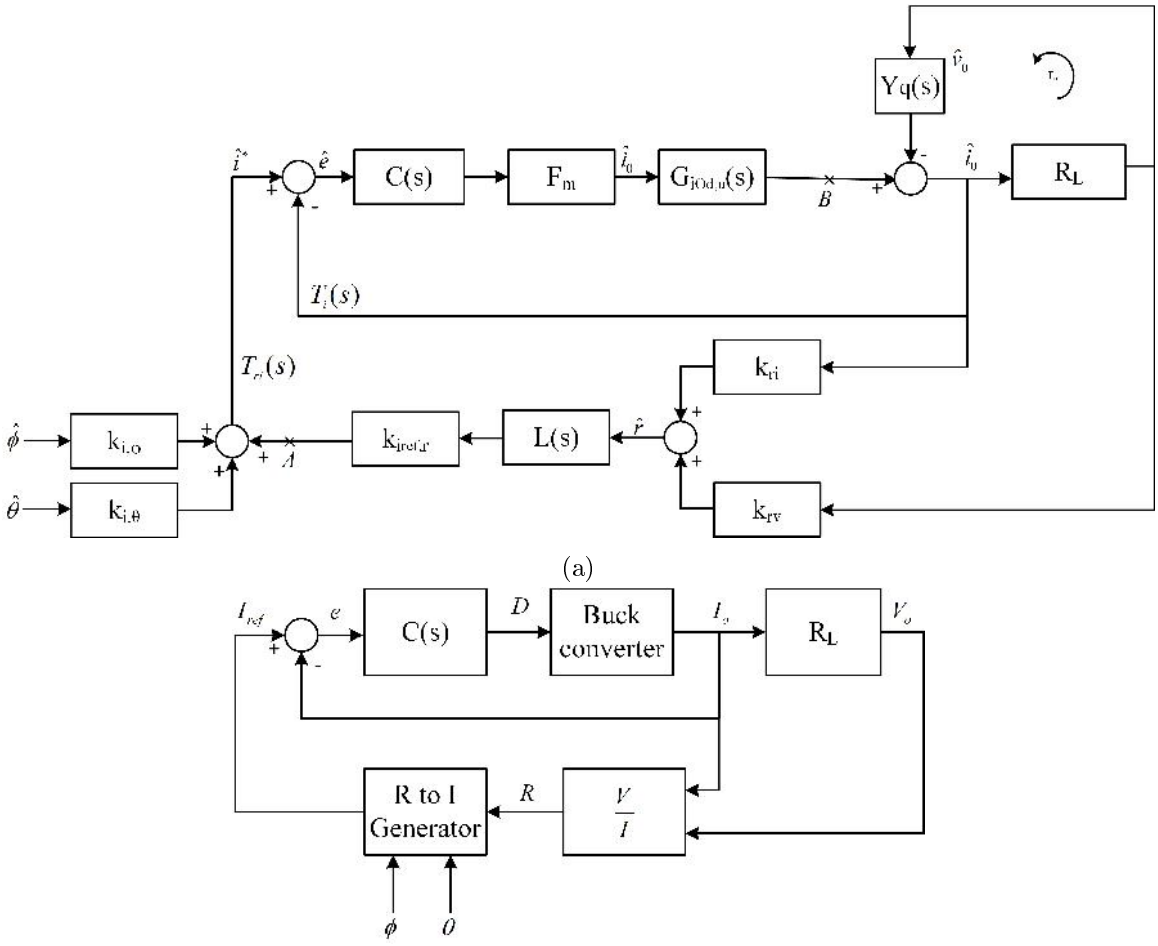


Figure 3-5: Modeling of RS-CRC (a) Small-signal block diagram (b) Large-signal block diagram

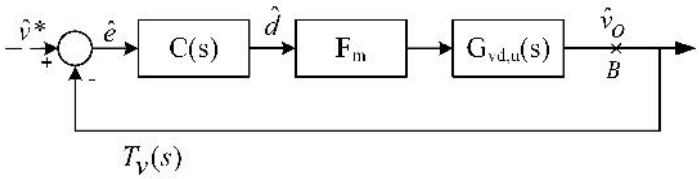


Figure 3-6: CS-VRC system small-signal block diagram for CC load

3.3 Small-signal analysis of SAS with CC load

3.3.1 CS-VRC configuration

In the CS-VRC topology, the block diagram of the small-signal model is shown in Fig. 3-6. Due to the independent voltage loop in the CS-VRC SAS system, the CC load model can be operated and interpreted as shown below.

$$T_v(s) = F_m C(s) G_{vd}(s) \tag{3.24}$$

and

$$T_{iv}(s) = 0 \tag{3.25}$$

Thus, only the inner-loop exists, and no dynamics appear in the loop, and the bode plot became as shown in Fig. 3-7a. It demonstrates that the dynamics of the CS-VRC system are independent of the operating point under CC load.

3.3.2 RS-VRC configuration

Due to control loop confliction, CC loads are not compatible with current reference control VS-CRC and RS-CRC topologies. Furthermore, CS-VRC and RS-VRC topology can be modeled with the CC loads. Their block diagrams of the small-signal model are shown in Fig. 3-8 and loop gain equation can be derived as

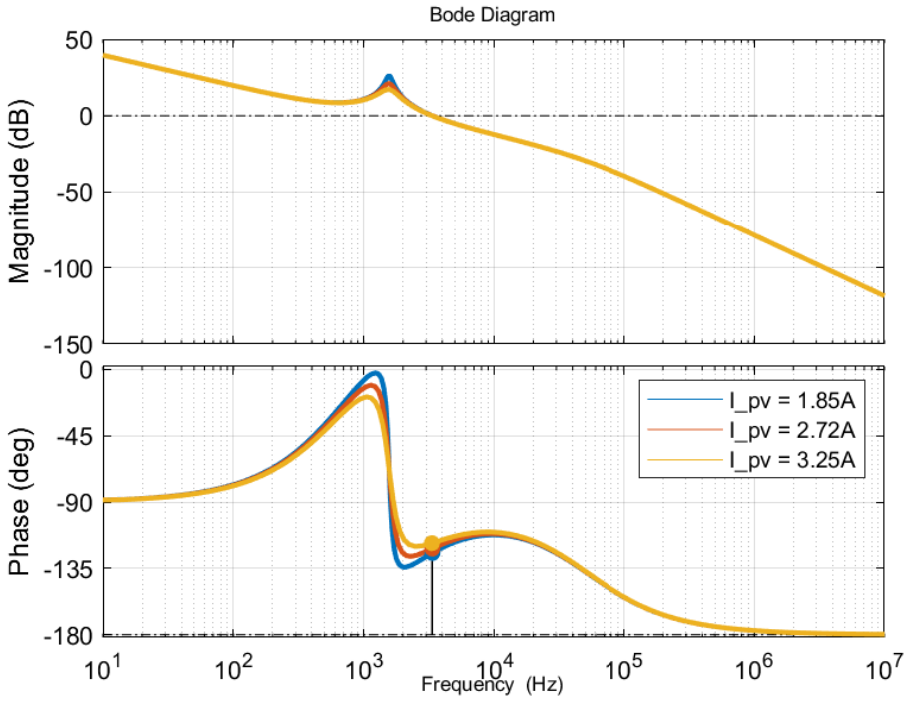
$$T_v(s) = F_m C(s) G_{vd}(s) \tag{3.26}$$

and

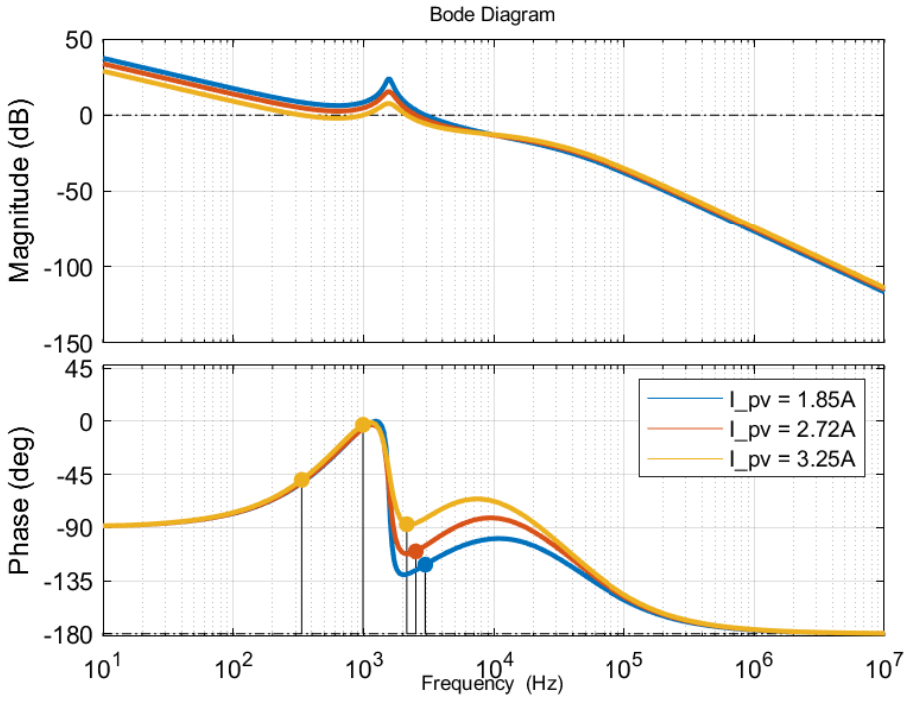
$$T_{rv}(s) = F_m C(s) G_{vd}(s) k_{v_{ref},r} k_{rv} L(s), \tag{3.27}$$

respectively. Thus,

$$T_B(s) = F_m C(s) G_{vd}(s) \left(1 - k_{v_{ref},r} k_{rv} L(s)\right) \tag{3.28}$$



(a)



(b)

Figure 3-7: Bode diagrams of the overall loop gain with CC load (a) CS-VRC (b) RS-VRC

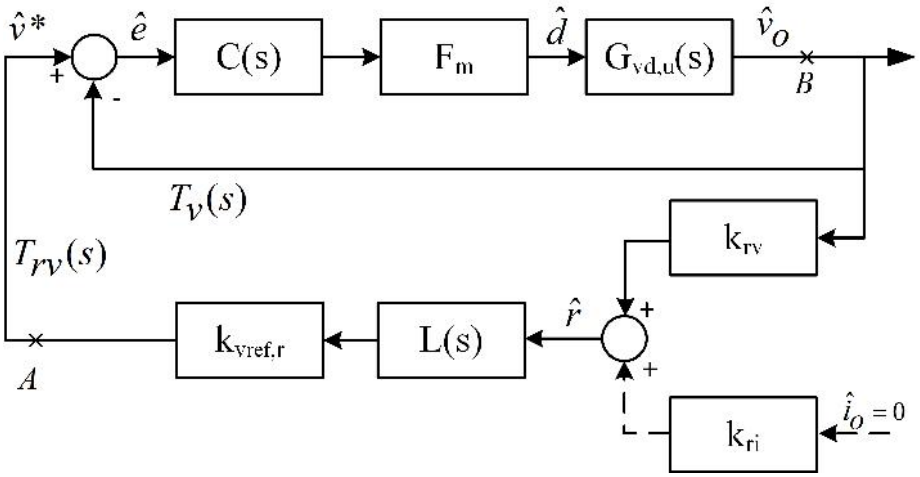


Figure 3-8: RS-VRC system small-signal block diagram for CC load

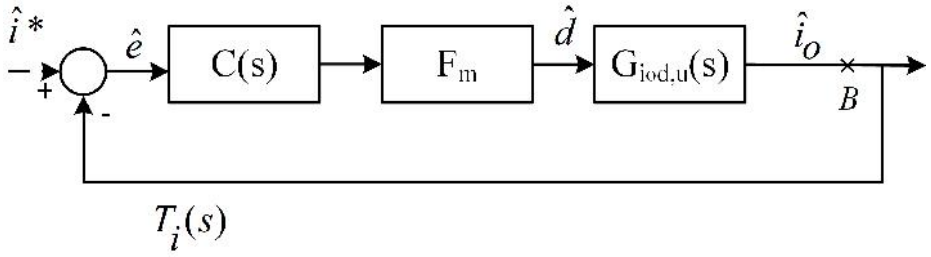


Figure 3-9: VS-CRC system small-signal block diagram for CV load

However, the outer loop dynamics exist and it is not nullified in RS-VRC.

$$k_{rv} = \frac{1}{I_o}, \tag{3.29}$$

Thus, the bode plot became as shown in Fig. 3-7a. It demonstrates that the dynamics of the RS-VRC system are affected by the operating point under CC load.

3.4 Small-signal analysis of SAS with CV load

3.4.1 VS-CRC configuration

In the VS-CRC topology, the small-signal block diagram is shown in Fig. 3-9. Then the loop gain equations become

$$T_v(s) = F_m C(s) G_{i_o d}(s) \tag{3.30}$$

and

$$T_{iv}(s) = 0, \tag{3.31}$$

respectively. Similar to the CS-VRC with CC load, only the inner-loop is exist and no dynamics appears in the loop and the bode plot became same with Fig. 3-10a. It also reflect that the dynamics of the VS-CRC system are independent of the operating point under CV load.

3.4.2 RS-CRC configuration

In the RS-CRC topology, the small-signal model block diagram can be modified as Fig. 3-11, and loop gain can be derived as

$$T_i(s) = F_m C(s) G_{i_od}(s) \tag{3.32}$$

and

$$T_{ri}(s) = F_m C(s) G_{i_od}(s) L(s) k_{i_{ref},r} k_{ri}. \tag{3.33}$$

Thus,

$$T_B(s) = F_m C(s) G_{i_od}(s) \left(1 - k_{i_{ref},r} k_{ri} L(s)\right) \tag{3.34}$$

Under this condition, it should be note that there is outer loop interactions in VS-CRC while the outer loop dynamics are not nullified in RS-CRC.

$$k_{ri} = -\frac{V_o}{i_o^2}. \tag{3.35}$$

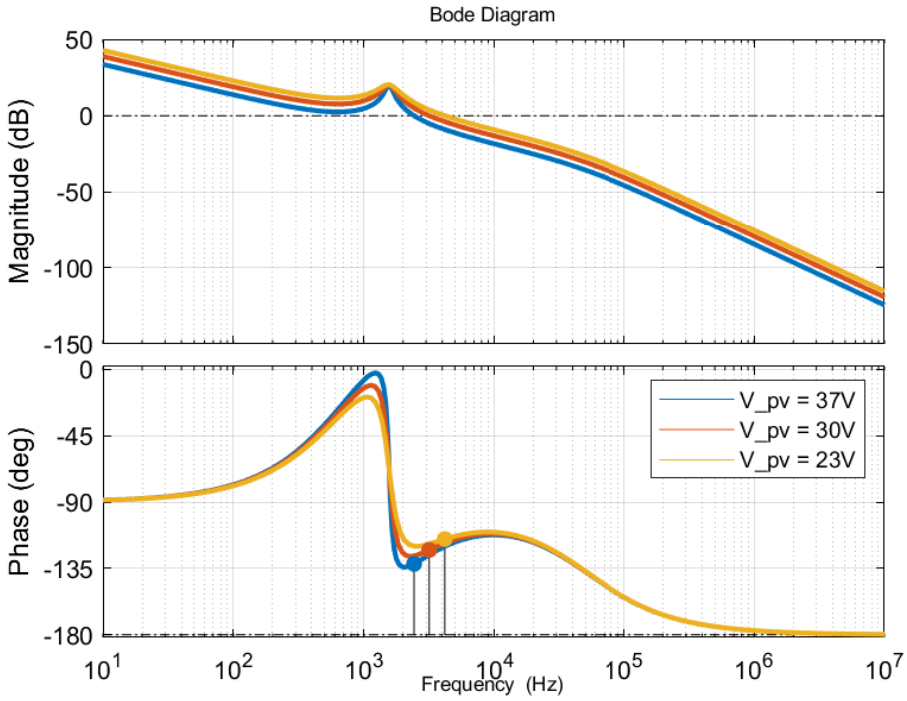
Thus, the bode plot became as shown in Fig. 3-10b. It also demonstrates that the dynamics of the RS-CRC system are affected by the operating point under CV load.

3.5 Performance comparison

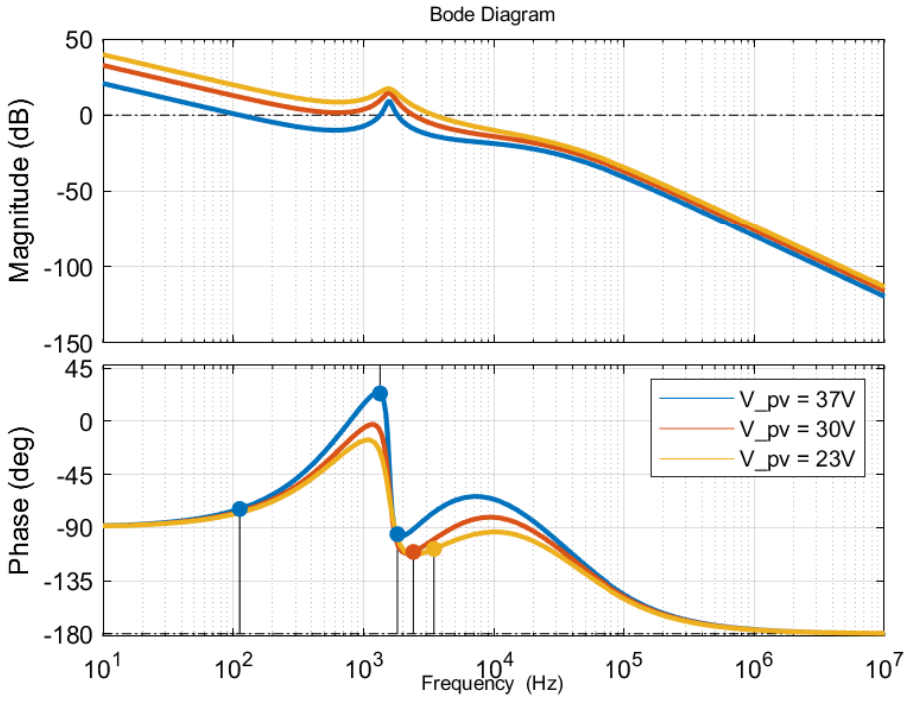
3.5.1 Design specification

According to the available lab facilities and development convenience, the target system is chosen as Table 3.1. MSX120 PV module with parameters in Table 3.2 is well-matched with the power plant parameters.

The buck converter in Fig. 3-12 is used for this research. Because the SAS output voltage and current are varied from zero to V_{oc} and I_{sc}, respectively, thus buck operation provides such a behavior. Further, the buck converter has a second-order output filter which delivers a low ripple output. The maximum duty cycle should be calculated by considering



(a)



(b)

Figure 3-10: Bode diagrams of the overall loop gain with CV load (a) VS-CRC (b) RS-CRC

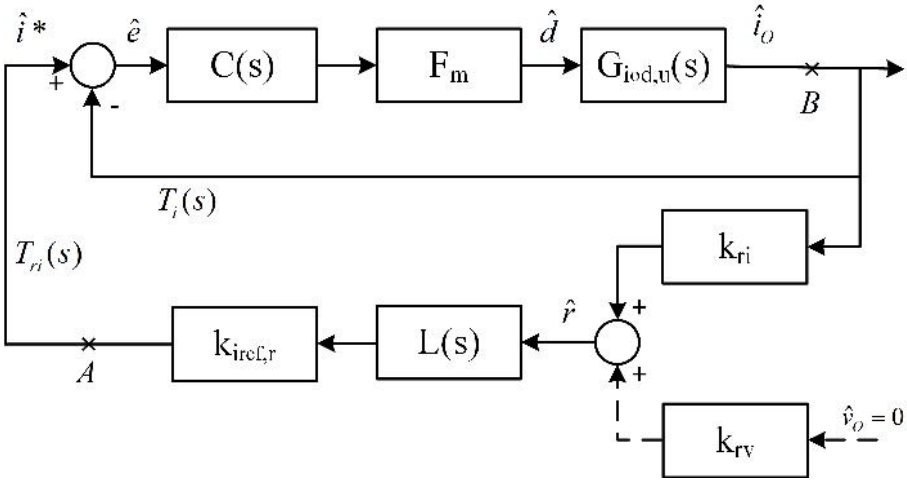


Figure 3-11: RS-CRC system small-signal block diagram for CV load

Table 3.1: Power plant parameters

Parameter	Value
Input voltage (V_s)	60 V
Expected output voltage (V_o)	50 V
Expected output current ($I_{o(max)}$)	4 A
Switching frequency (f_{sw})	100 kHz
Efficiency (η)	90 %
Allowed voltage ripple (ΔV_{out})	1 %
Allowed inductor ripple ($\Delta I_{L\%}$)	10 %
Target PV module	MSX120
Digital Controller	TMS320F28379D

Table 3.2: PV module parameters (MSX120) [8]

Parameter	Value
P_{Max}	120 W
V_{oc}	42.1 V
I_{sc}	3.87 A
V_{MPP}	33.7 V
I_{MPP}	3.56 A

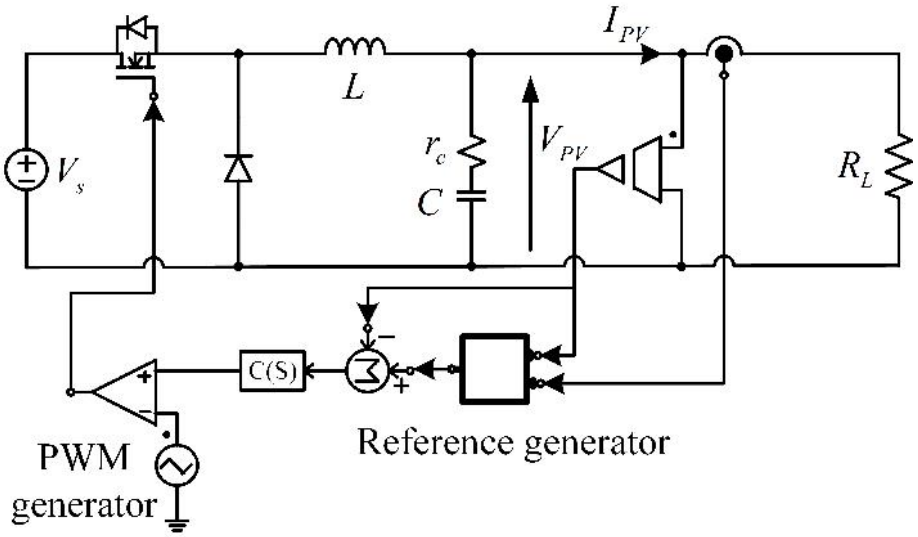


Figure 3-12: Buck converter schematic

the expected efficiency (η) to start the calculation.

$$D_{max} = \frac{V_{out}}{\eta V_s} = 0.93 \tag{3.36}$$

The MPPT loads are highly sensitive to the ripple voltage; thus, inductor ripple current is limited to 10%. Then

$$\Delta I_L = I_o \Delta I_{L\%} = 0.4A \tag{3.37}$$

The inductance can be calculated as

$$L = \frac{V_{out}(V_s - V_{out})}{\Delta I_L F_{sw} V_s} = 208\mu H \approx 210\mu H \tag{3.38}$$

The output capacitance can be calculated as

$$C = \frac{\Delta I_L}{8 F_{sw} \Delta V_{out}} = 50\mu F \tag{3.39}$$

The rating of the freewheeling diode ratings can be calculated as follows. The forward current becomes

$$I_f = I_{o(max)}(1 + D) = 280mA \tag{3.40}$$

and power dissipation

$$P_D = I_f V_f = 140mW. \tag{3.41}$$

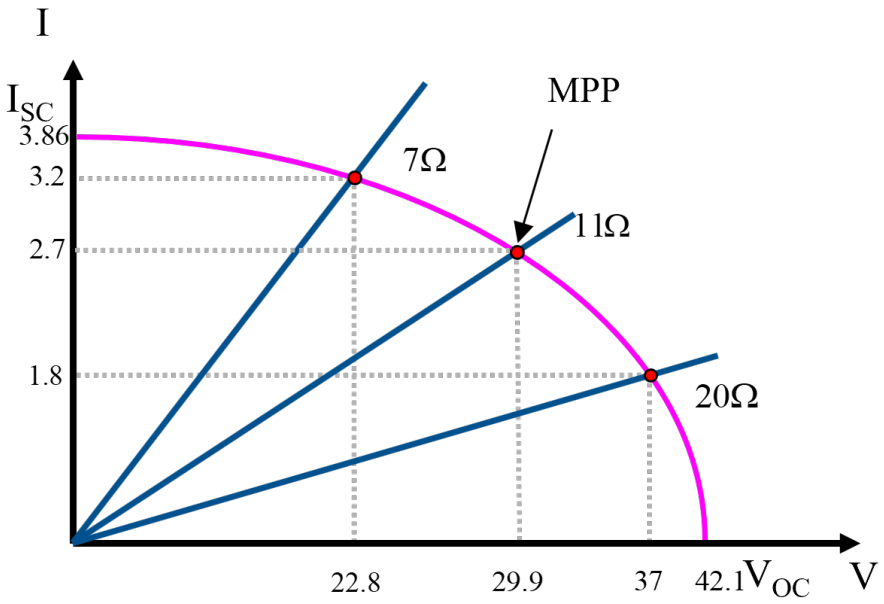


Figure 3-13: Operating point and load resistance set-up for verification on the approximate PV model curve

Here, V_f is taken as 0.5V for Y2010DN schottky diode. Converter switching MOSFET is chosen by considering above 1.5 times input voltage and minimum reverse recovery time. An N-Channel Onsemi MOSFET FDP150N10 has the rating of 100V for V_{DS}, 57A for I_D, and 41ns for t_{rr},thus it is finally chosen.

3.5.2 Frequency domain simulation

For frequency-domain simulations, subsystem blocks are arranged by MATLAB Simulink according to block diagrams in Figs. 3-1a, 3-3a, 3-4a, and 3-5a. The parameters of the buck converter and controller have listed in Table 3.3. The controller uses the type III compensator C(s) of expression

$$C(s) = \frac{k_u}{s} \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{3.42}$$

where k_u is the gain, ω_{z1} and,u ω_{z2} are real zeros, ω_{p1} and ω_{p2} are real poles. According to actual PV module specifications in Table 3.2, an elliptical approximate PV curve is generated with the same open-circuit voltage and short circuit current as shown in Fig. 3-13. The optimal controller design is demonstrated in different way, but k-factor method [5] and Christophe Basso method [89] are much popular. In this both case, Type-III controller

Table 3.3: Converter components and Type III controller parameters

Parameter	Value	Unit	Parameter	Value	Unit
V_s	60	V	ω_{z1}	4.4	krad/s
L	210	μH	ω_{z2}	8.8	krad/s
C	47	μF	ω_{p1}	314	krad/s
r_c	3.1	$m\Omega$	ω_{p2}	6.89	Mrad/s
k_u(VRC)	50	rad/s	ω_s	628.3	krad/s
k_u(CRC)	550	rad/s	f_s	100	kHz

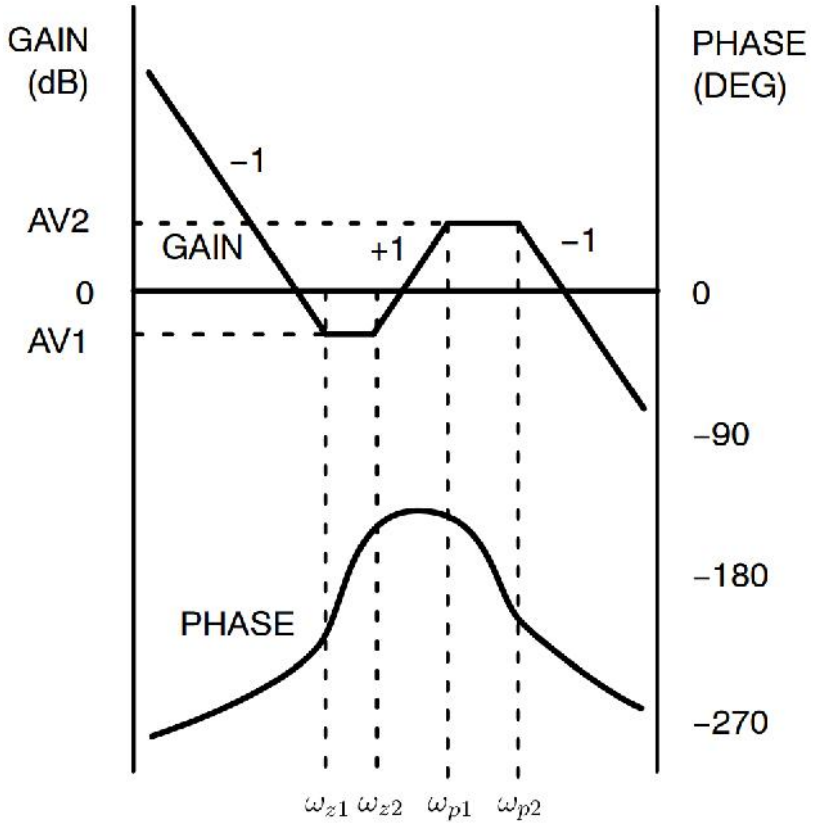


Figure 3-14: Frequency response of Type-III controller [5]

provides switch mode power converter related response which need to increase the phase margin over the operating bandwidth and suppress the phase beyond the f_{sw}. The Fig. 3-14 shows the superior transient response of the controller. 3-15 In this circuit, the network provides a pole at the origin with two zero-pole pairs. It shows how the low-frequency gain decreases at -20 dB/decade (-1 slope) due to the origin (integrator) pole. The gain becomes constant between the two zero frequencies, ω_{z1} and ω_{z2} and they are located below the

cut-off frequency. After ω_{z2}, the effects of second zero cause the gain to increase at +20 dB/decade (+1 slope) until approaching ω_{p1}. It is flat again after ω_{p1} and boosts the phase margin near the crossover frequency. After ω_{p2}, the magnitude response decreases at a rate of -20 dB/decade (-1 slope) and suppress the phase of the f_{sw}. Generally, ω_{p2} should be lower than $0.5f_{sw}$ for better f_{sw} immunity. The closed-loop compensation crossover should occur in between ω_{z2} and ω_{p1} for best results. The response of the type-III controller can be compared as shown in Fig. 3-15.

Three load resistance, 7Ω, 11Ω, and 20Ω, are chosen to test the stability of the current segment, MPP point, and voltage segment point, respectively. For each condition, Bode plots for the inner loop gain $T_v(s)$ and $T_i(s)$ are shown in Fig. 3-16, describing system stability without considering outer loop interactions. Bode plots for the overall loop gain $T_B(s)$ for various SAS architectures are presented in Fig. 3-17 and Fig. 3-18. In the CS-VRC system in Fig. 3-17a, when the load resistance is decreased, the operating point moves towards the current source segment, and the loop gain increases significantly. This results in an increment in gain cross-over frequency and a loss of the phase margin. On the other hand, the RS-VRC in Fig. 3-17b confirms that the loop gain change is not significant for the three loads. The CRC configuration in Fig. 3-18a and Fig. 3-18b show that overall loop characteristics are load-dependent. However, RS-CRC in Fig. 3-18b is far less sensitive to load than VS-CRC in Fig. 3-18a, and its overall loop gain behaves similarly to the inner loop gain in Fig. 3-16b.

As further analysis, the root locus of each system can be considered. The root-locus of four SAS configurations are plotted in Fig. 3-19 to Fig. 3-22. For example, the CS-VRC system can be considered for the root locus equation. Here, its denominator of overall closed-loop gain function with gain sweeper (k) can be written as

$$T_B(s) = 1 + k(F_m C(s) G_{vd}(s) K_1(s)). \tag{3.43}$$

Thus, it is possible to plot the root locus for different loads. It also follows the trend of the bode plots in which the RS-based system always shows stable negative roots, but roots are moving in the right-land plane, which causes an unstable response in CS-VRC and VS-CRC configuration.

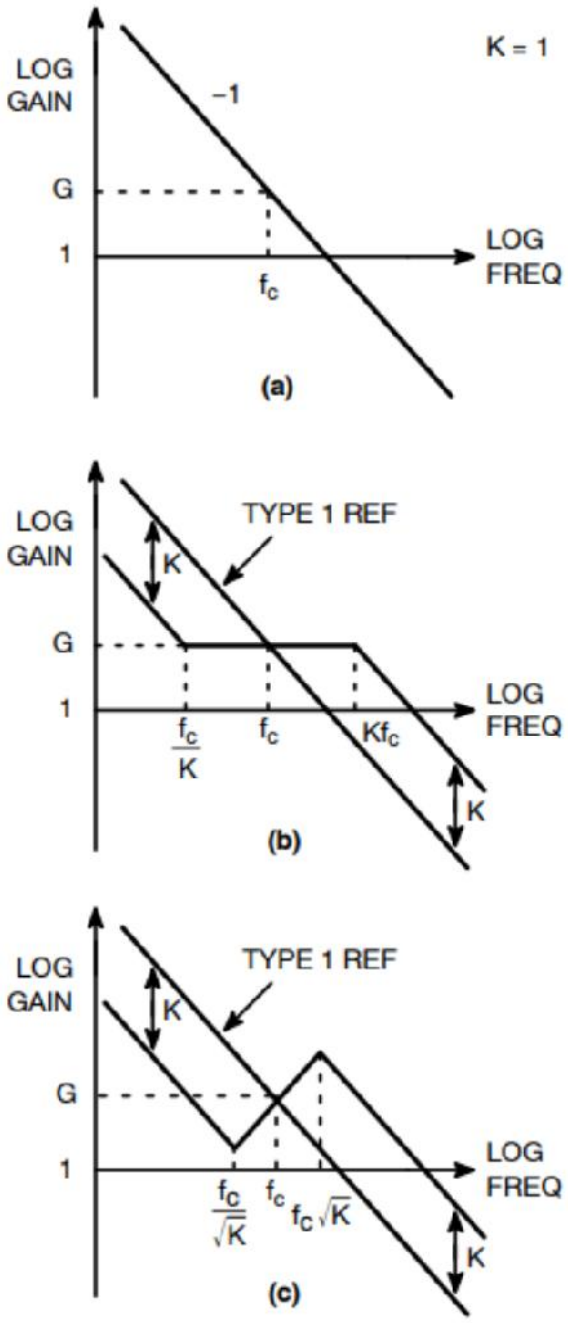
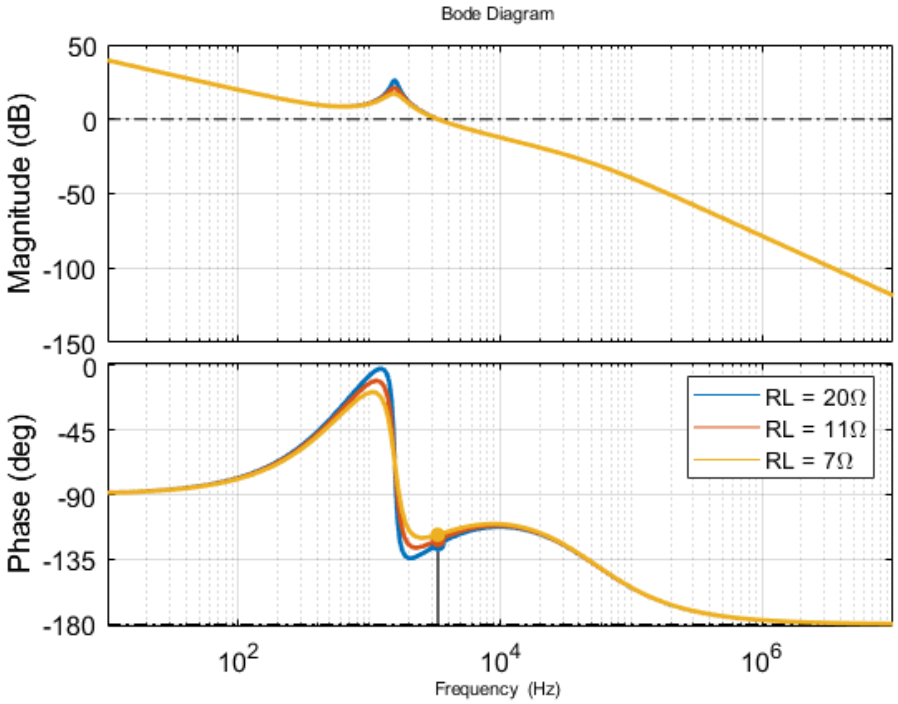
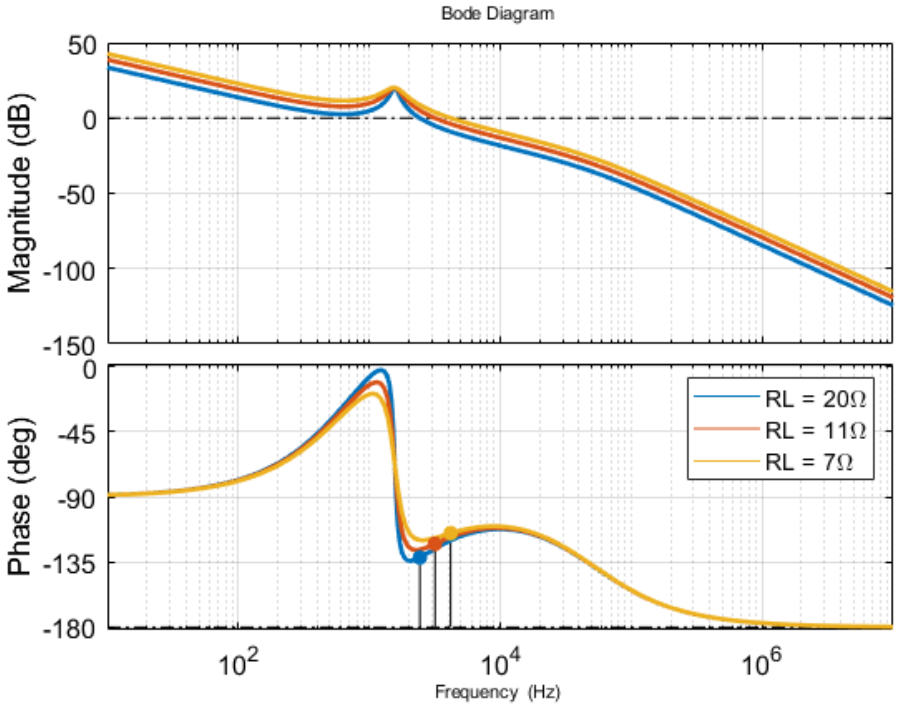


Figure 3-15: Comparison of bode plot characteristics of each controller in relation to the K factor [5] (a) Type-I controller (b) Type-II controller (c) Type-III controller

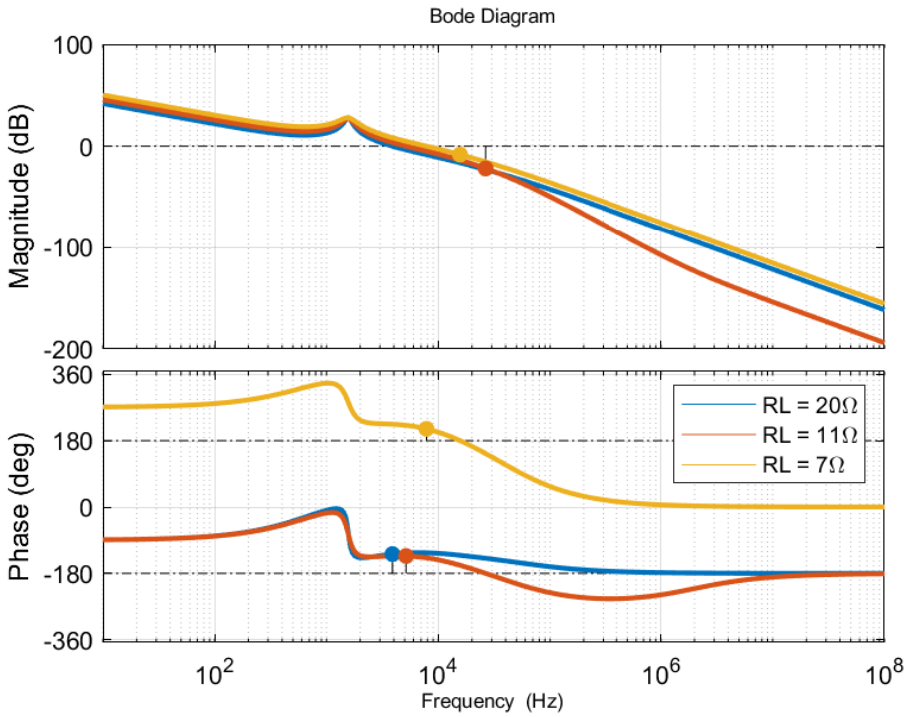


(a)

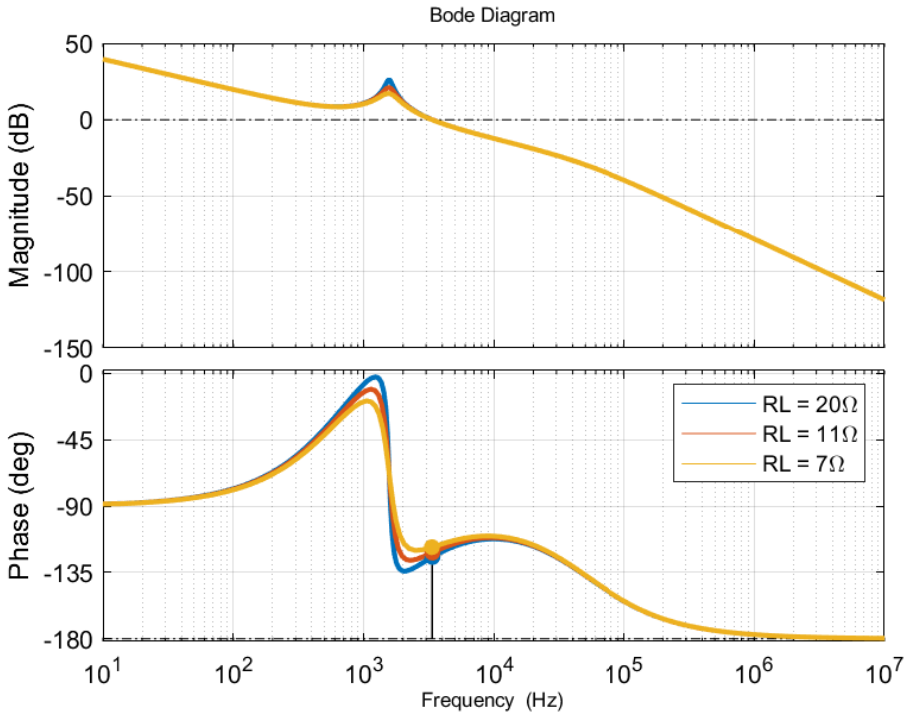


(b)

Figure 3-16: Bode diagrams of the inner loop gain (a) $T_v(s)$ in VRC (b) $T_i(s)$ in CRC

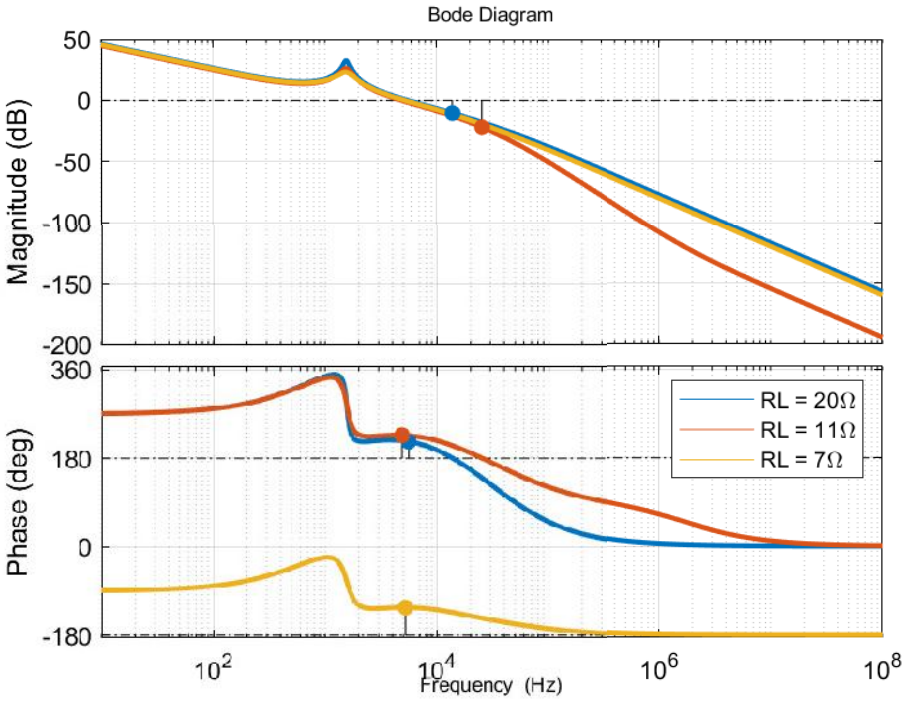


(a)

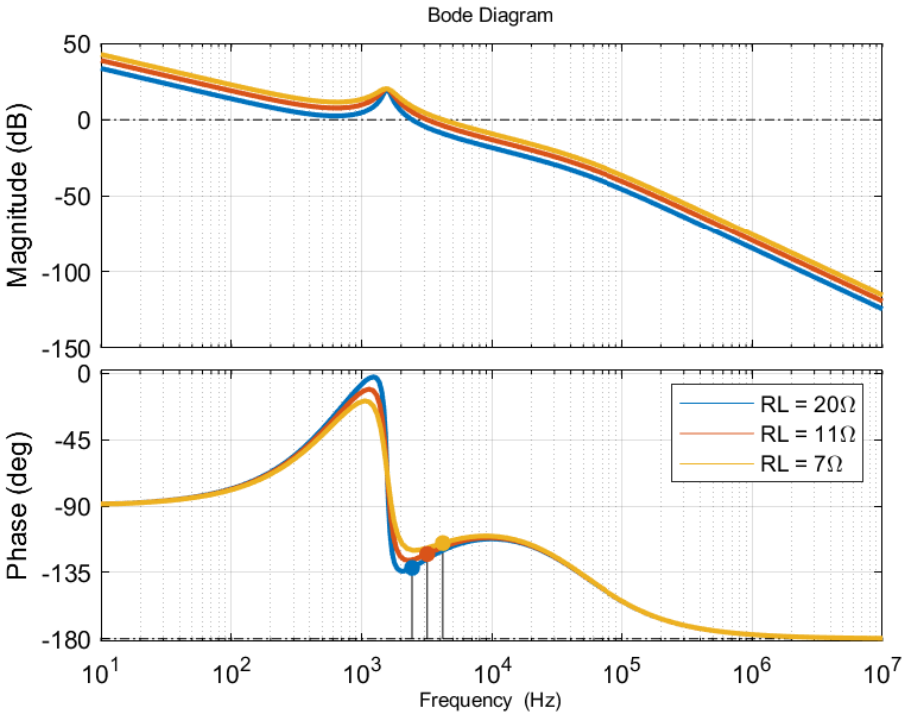


(b)

Figure 3-17: Bode diagrams of the overall loop gain in VRC system $T_B(s)$ (a)CS-VRC (b)RS-VRC

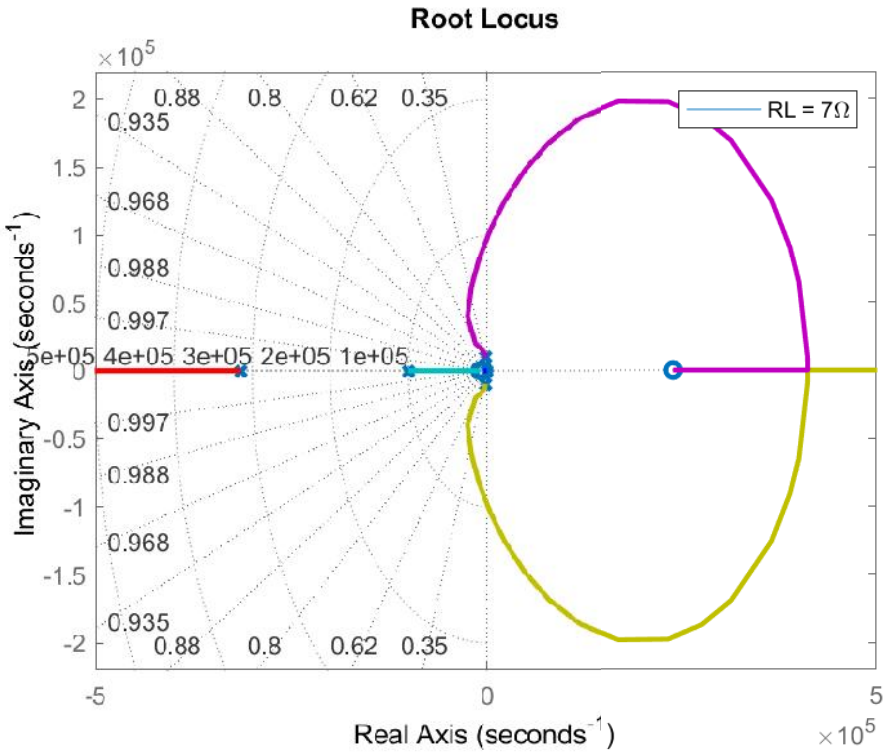


(a)

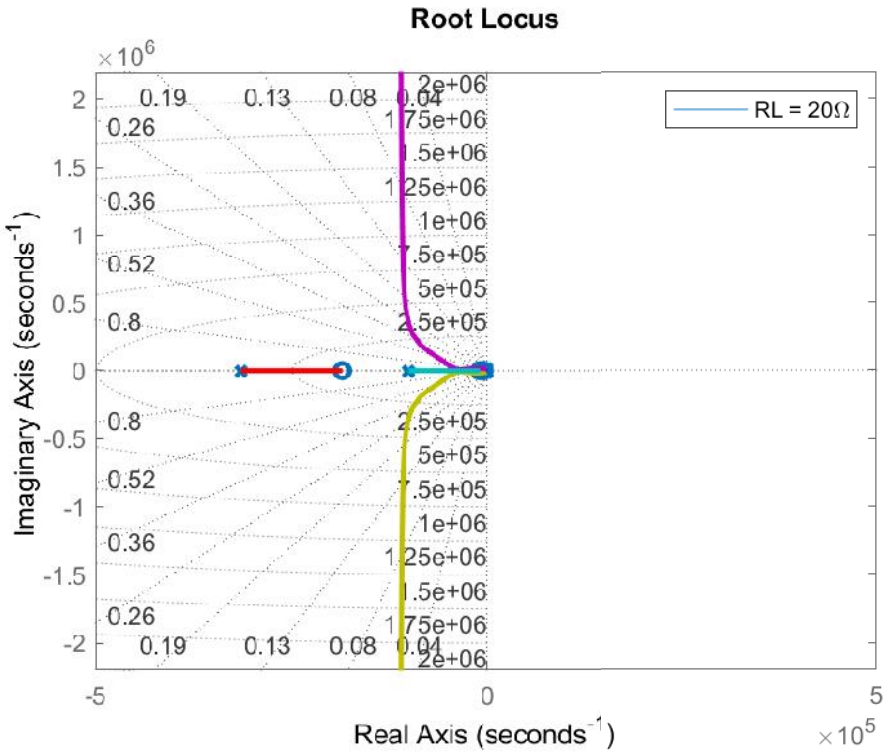


(b)

Figure 3-18: Bode diagrams of the overall loop gain in CRC system $T_B(s)$ (a)VS-CRC (b)RS-CRC

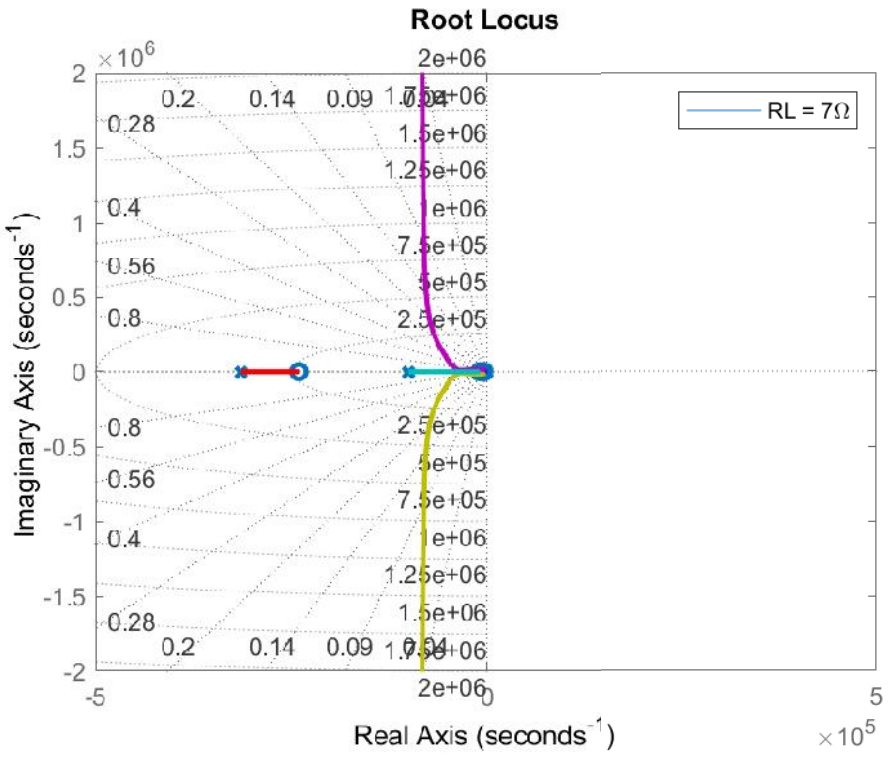


(a)

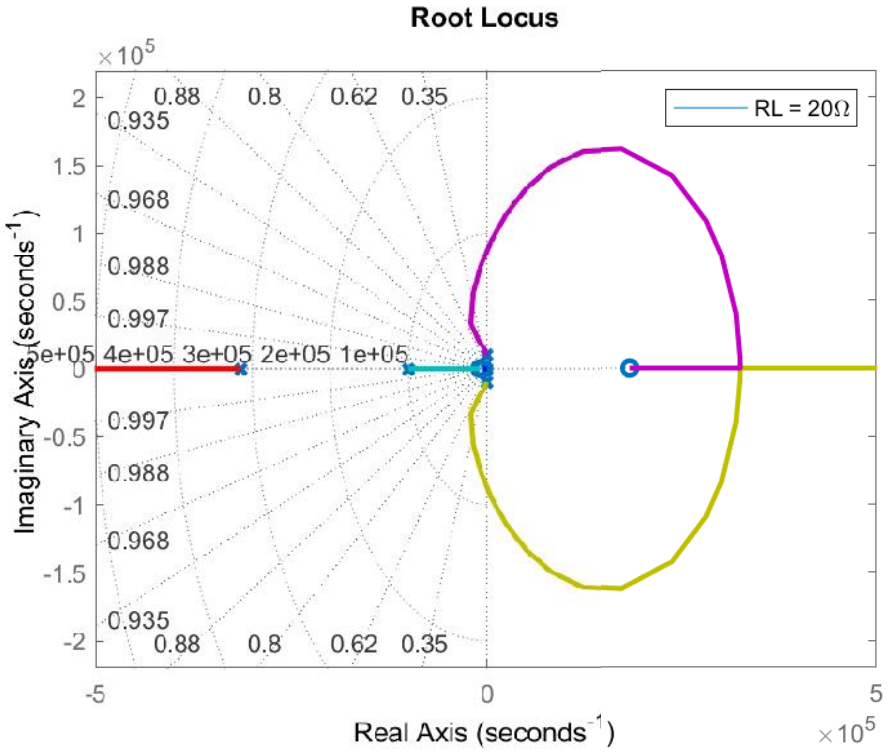


(b)

Figure 3-19: Root-locus of the overall loop gain in CS-VRC system $T_B(s)$ (a) 7Ω load (b) 20Ω load

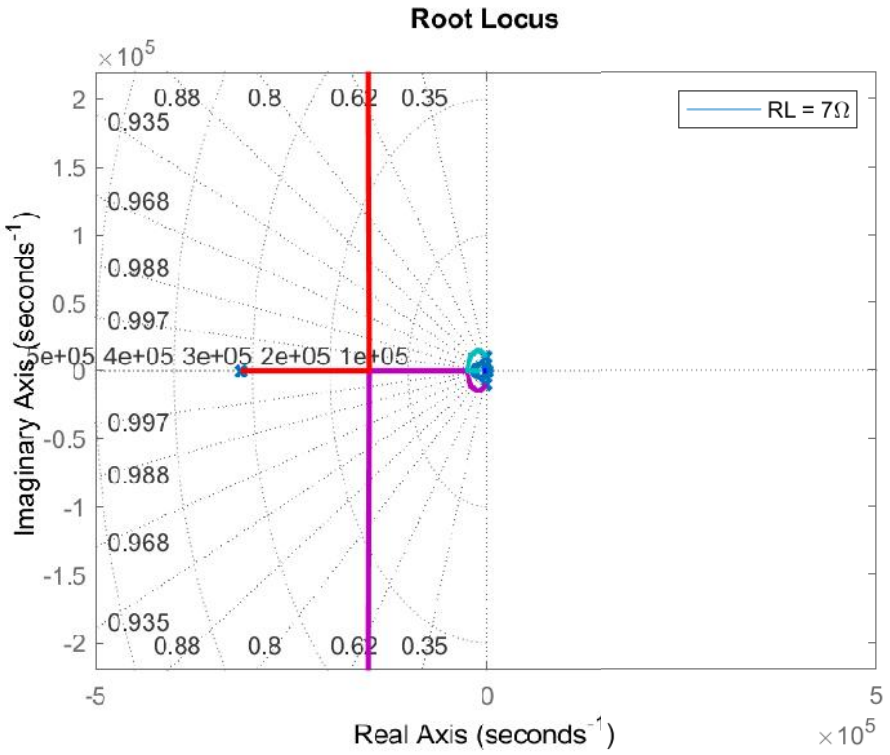


(a)

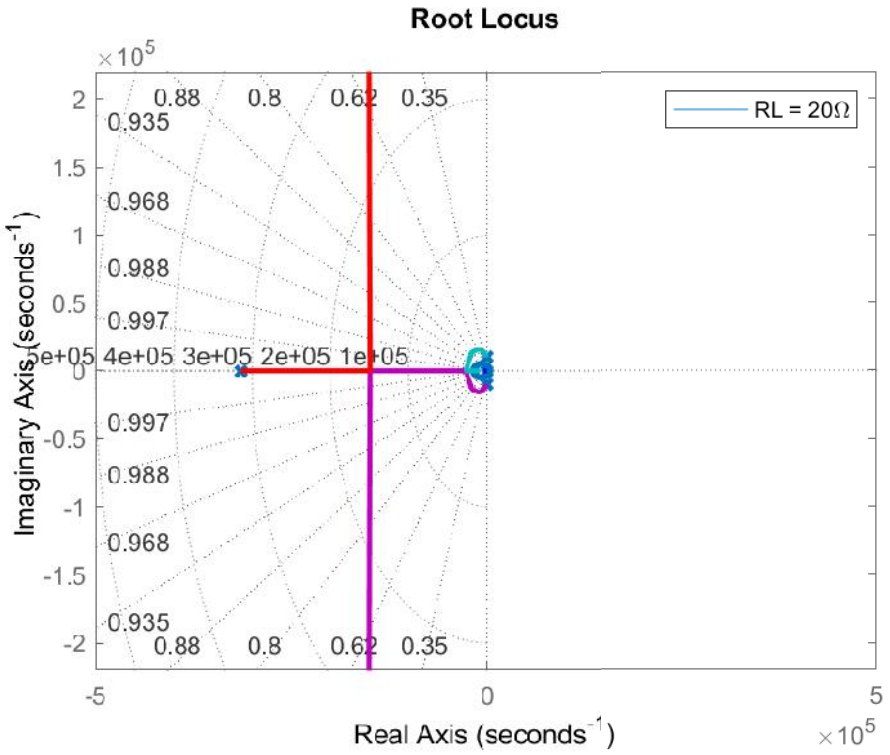


(b)

Figure 3-20: Root-locus of the overall loop gain in VS-CRC system $T_B(s)$ (a) 7Ω load (b) 20Ω load

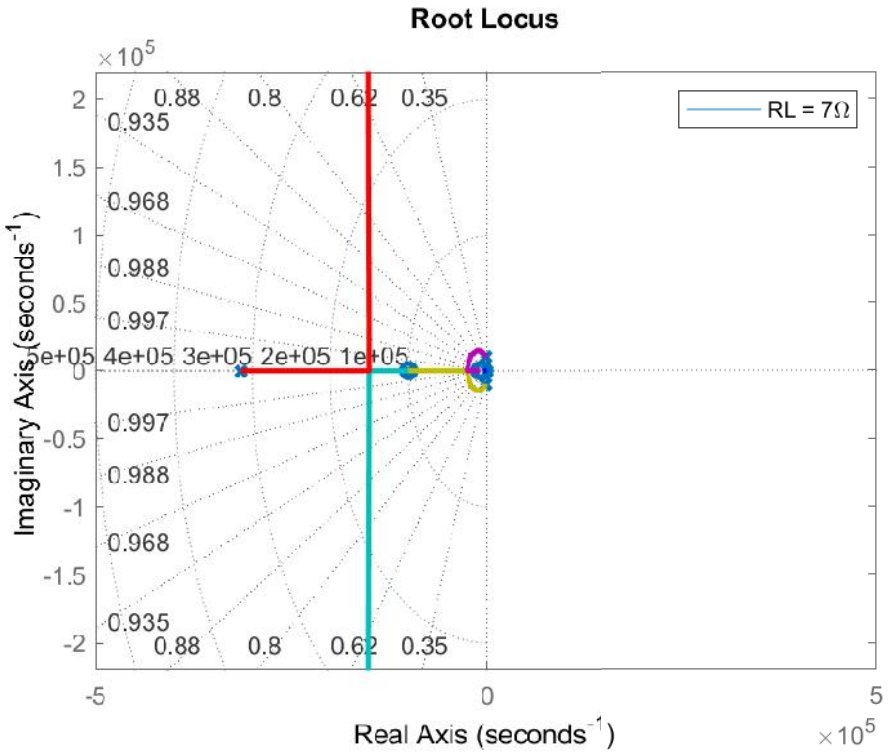


(a)

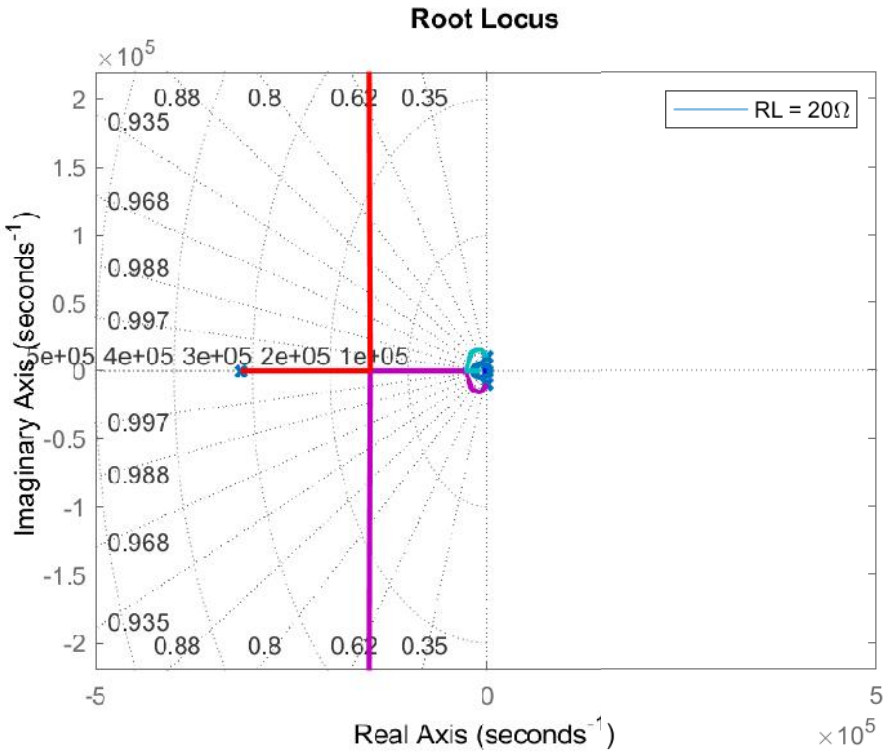


(b)

Figure 3-21: Root-locus of the overall loop gain in RS-VRC system $T_B(s)$ (a) 7Ω load (b) 20Ω load



(a)



(b)

Figure 3-22: Root-locus of the overall loop gain in RS-CRC system $T_B(s)$ (a) 7Ω load (b) 20Ω load

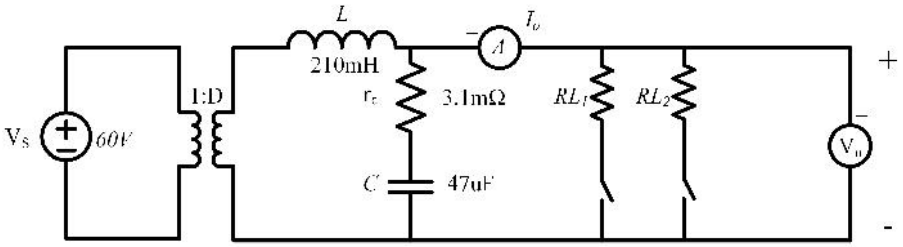


Figure 3-23: Buck converter average model

Table 3.4: Simulation results

Operating point	Current segment		MPP		Voltage segment	
System	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CS-VRC	1.9*	2.2	1.3*	0.7	0.2*	0.4
RS-VRC	0*	0.9	0*	1.0	0*	0.4
VS-CRC	0.8	0.3	1.5	0.8	10	9.3
RS-CRC	0.5	0.3	0.3	0.9	0.8	1.8

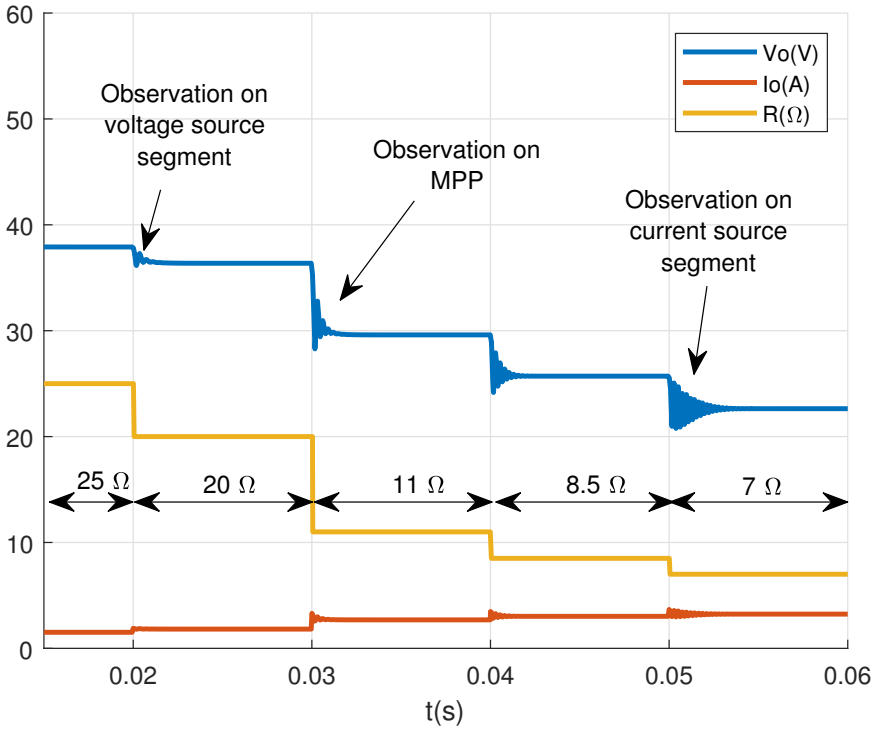
$*^*$ = undershoot

3.5.3 Time domain simulation

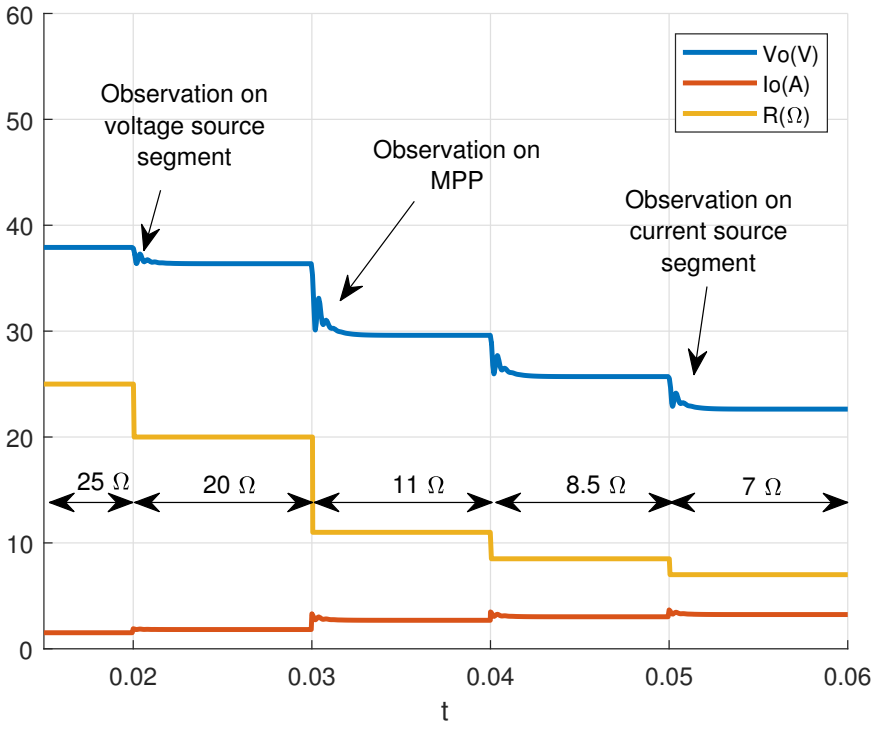
For the time-domain simulations, the PSIM schematic is implemented following Fig. 3-23. The buck average model [90] accelerates the simulation, and two load resistors in parallel give the load disturbance. By stepping the load resistance by around 40% at each operating point, the recovery waveform of the output voltage is presented in Fig. 3-24 and 3-25.

It should be noted that CRC systems are very much affected by the load changes in the voltage source segment, while VRC systems have the same issue in the current source segment. Consequently, the load resistance step-up test is performed for the CRC case, and the load resistance step-down test is applied for the VRC case. Step changes of load resistance area marked in Fig. 3-24 and 3-25. Fig. 3-26 and Table 3.4 summarize the dynamic performance depending on the operating point.

According to the theoretical analysis, the VRC system has a small phase margin for low resistive load. In the CS-VRC system in Fig. 3-24a, as the load decreases from 20Ω to 7Ω, the settling time is increased from 0.27ms to 2.1ms, and the phase margin is reduced, causing an undershoot in the output. Since the phase margin is not sufficient, the system shows under-damped oscillations in the condition of low resistance.

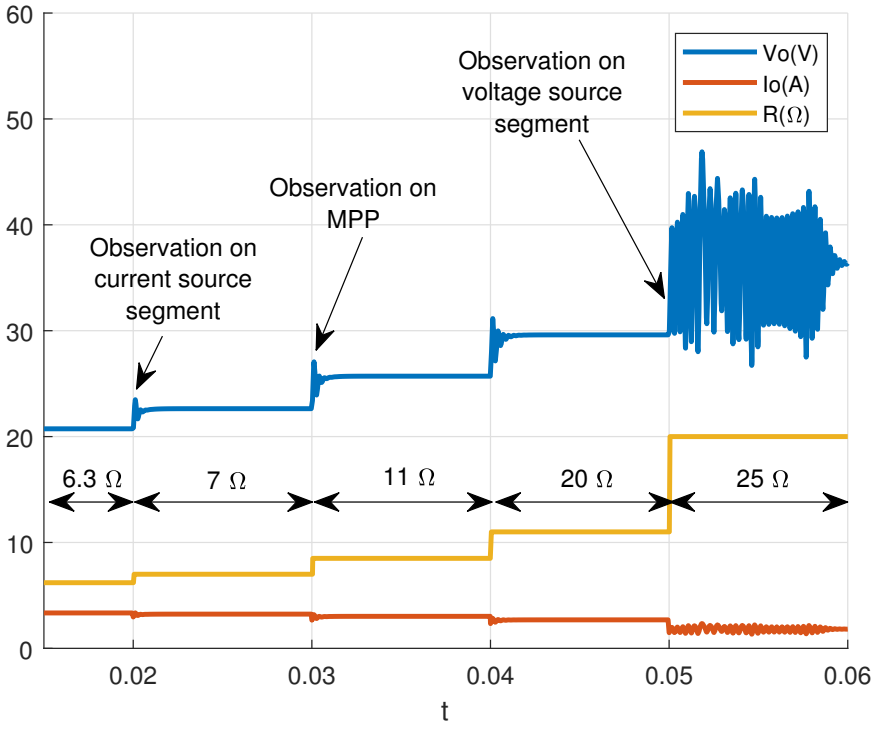


(a)

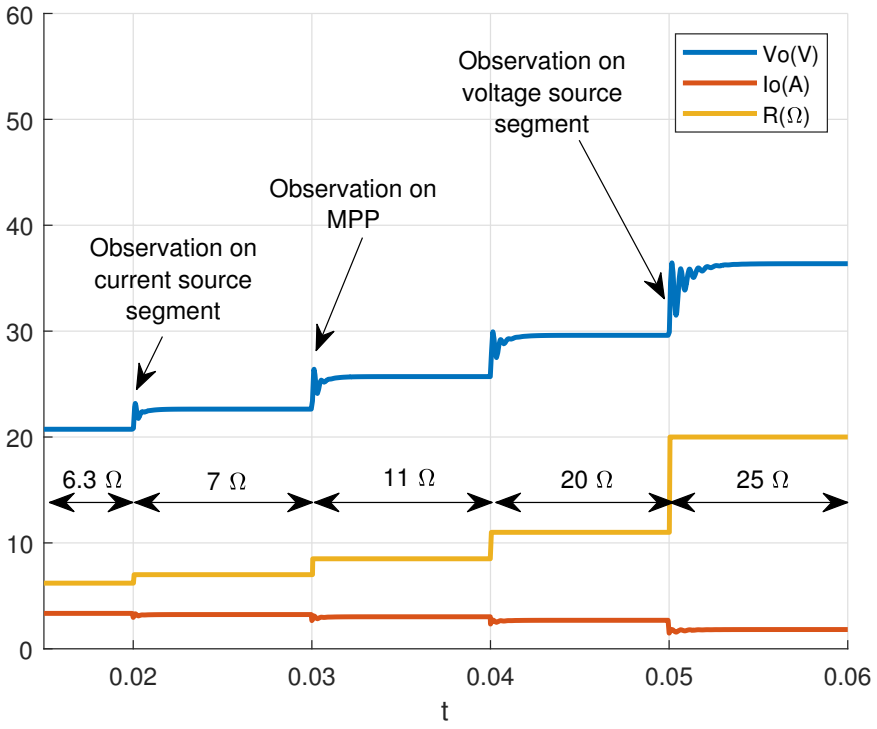


(b)

Figure 3-24: Step load response for different configurations in VRC (a)CS-VRC (b)RS-VRC

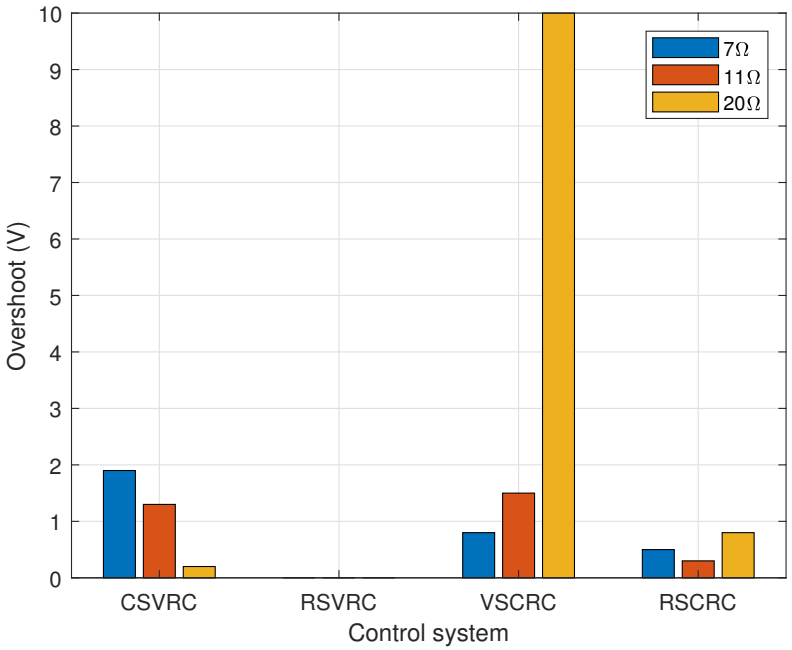


(a)

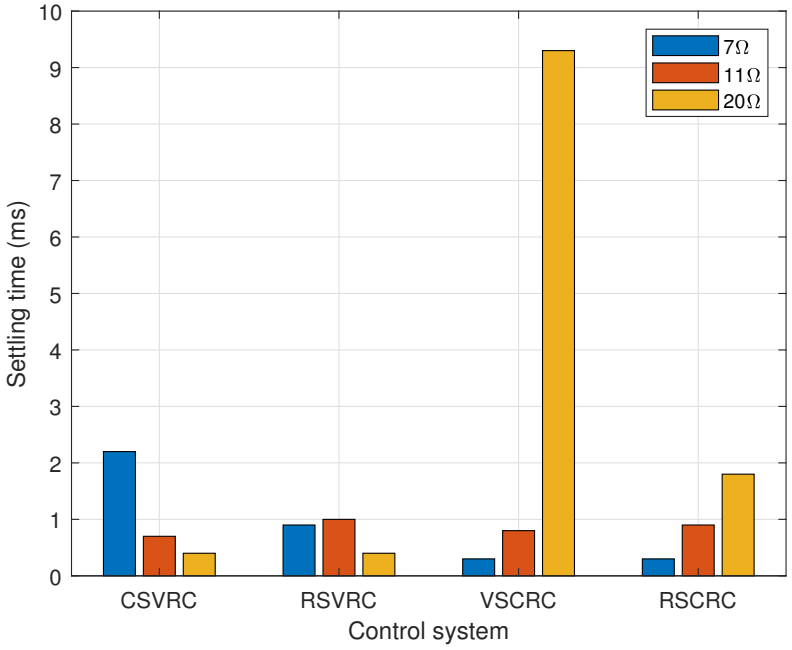


(b)

Figure 3-25: Step load response for different configurations in CRC (a)VS-CRC (b)RS-CRC



(a)



(b)

Figure 3-26: Simulation results (a)Overshoot (b)Settling time

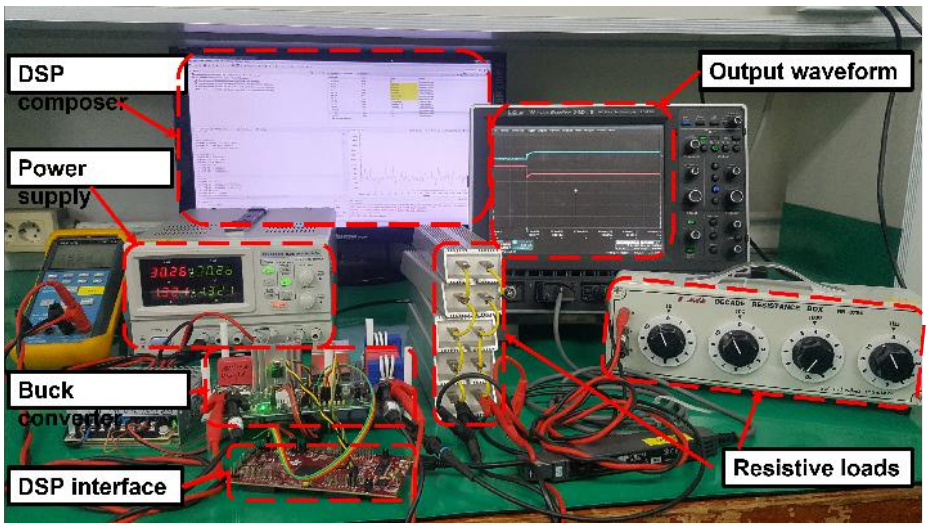


Figure 3-27: Hardware setup of SAS

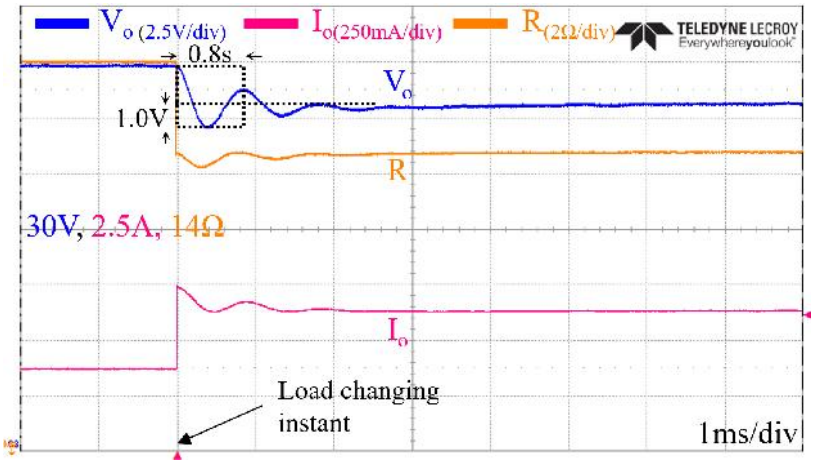
On the other hand, the response of the RS-VRC system in Fig. 3-24b shows that regardless of variations in operating points, the settling time changes only slightly from 0.3ms to 0.9ms without severe oscillations. This tendency matches well with the theoretical expectation on the operating point insensitivity of the RS-VRC configuration mentioned in section III.D.

Similarly, VS-CRC and RS-CRC systems are compared to demonstrate our theoretical predictions. In this case, the load resistance is tested in ascending order from 7Ω to 20Ω, considering a more stable operation in the voltage segment region. Fig. 3-25a and Fig. 3-25b show the output response, and the results are very similar to those of the VRC case. According to the duality in CS-VRC and VS-CRC configurations, the system stability has deteriorated in high resistance load, and RS-CRC is less sensitive to the load change than VS-CRC.

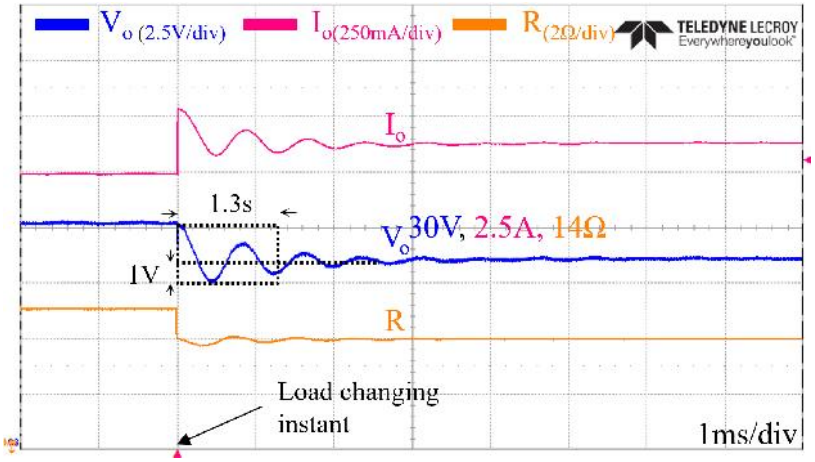
Even though RS-CRC shows similar trends to RS-VRC, its dynamic response is relatively sensitive to the operating point variations because the power stage transfer function has load-dependent dc-gain characteristics. Therefore, RS- VRC seems to be the best configuration in terms of load-independent dynamic characteristics. This confirms the validity of the comparison based on the small-signal analysis presented in this study

3.5.4 Experimental verification

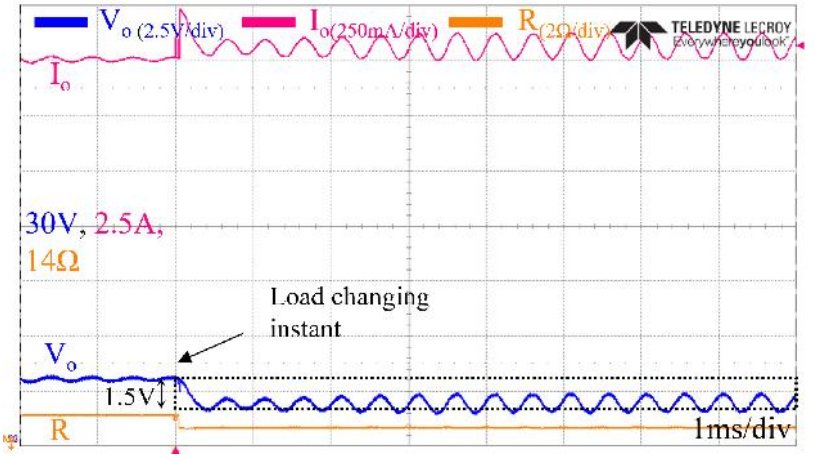
The SAS system consisting of a buck converter incorporated with a TMS320F28379D DSP controller for the hardware validation is shown in Fig. 3-27. Following simulation test



(a) $20\Omega \rightarrow 15\Omega$



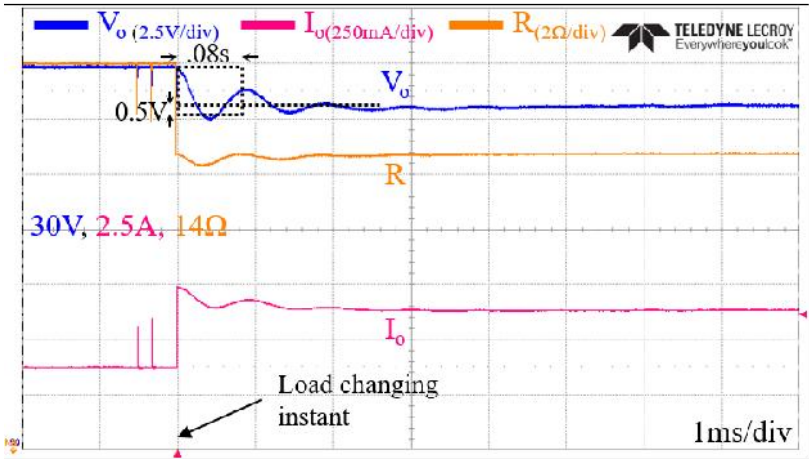
(b) $11\Omega \rightarrow 10\Omega$



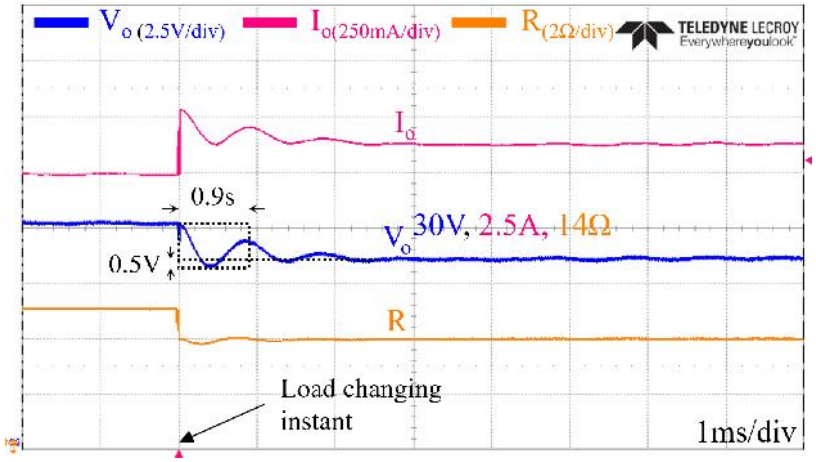
(c) $7\Omega \rightarrow 6.3\Omega$

Figure 3-28: Hardware step load change of CS-VRC system

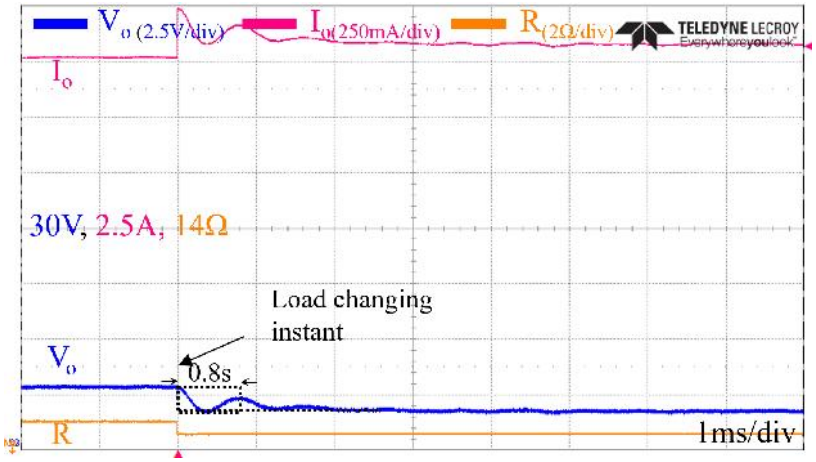
scenarios, step responses at the three operating points are tested. Here, two variable resistor loads are connected for making the step load change. Experimental results are shown from Fig. 3-28to 3-31, and its dynamic performance indices are summarized in Table 3.5.



(a) $20\Omega \rightarrow 15\Omega$

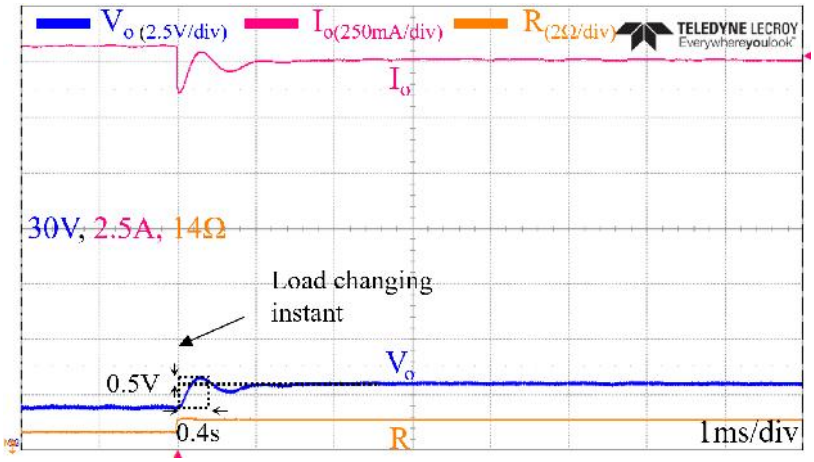


(b) $11\Omega \rightarrow 10\Omega$

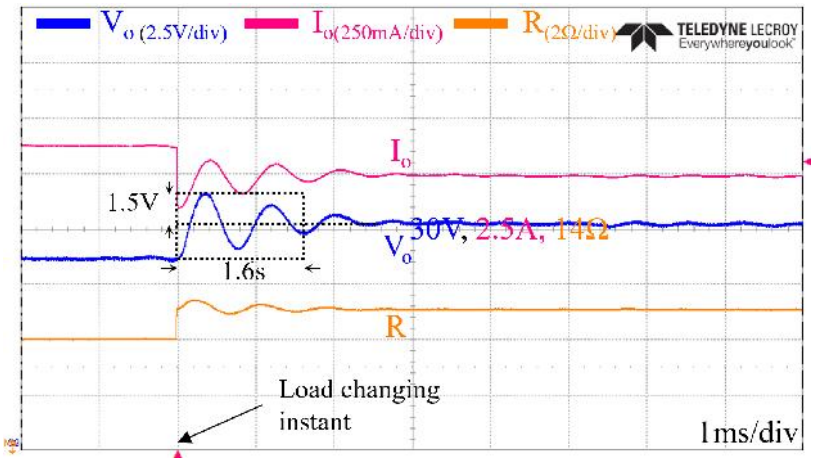


(c) $7\Omega \rightarrow 6.3\Omega$

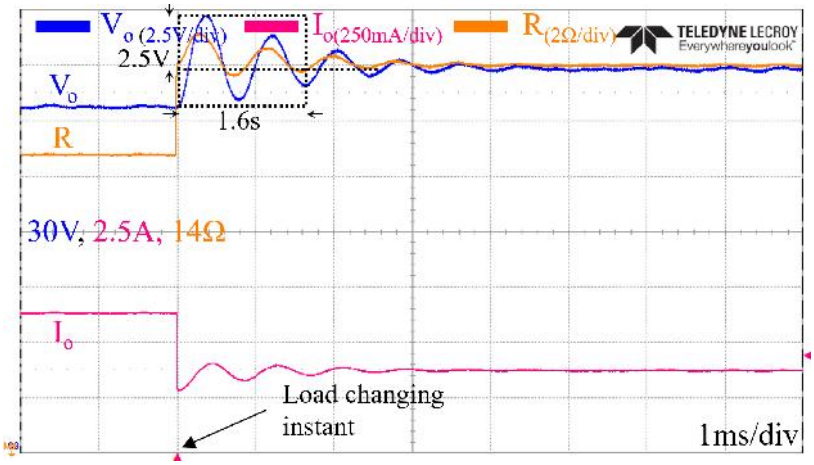
Figure 3-29: Hardware step load change of RS-VRC system



(a) 6.3Ω → 7Ω

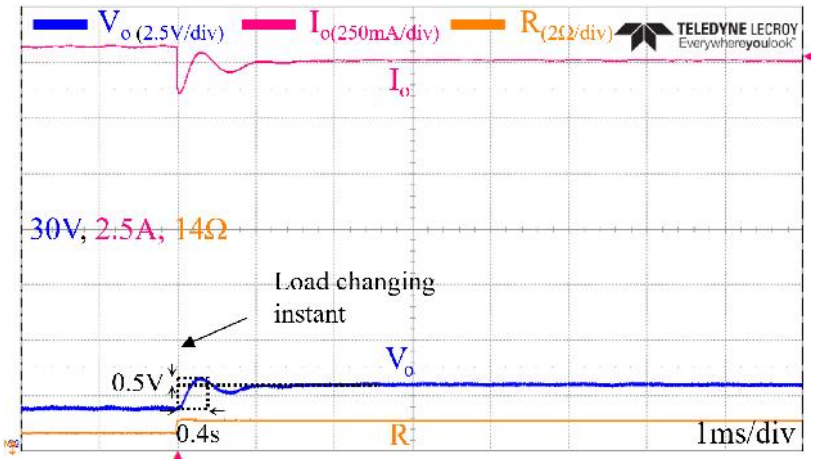


(b) 10Ω → 11Ω

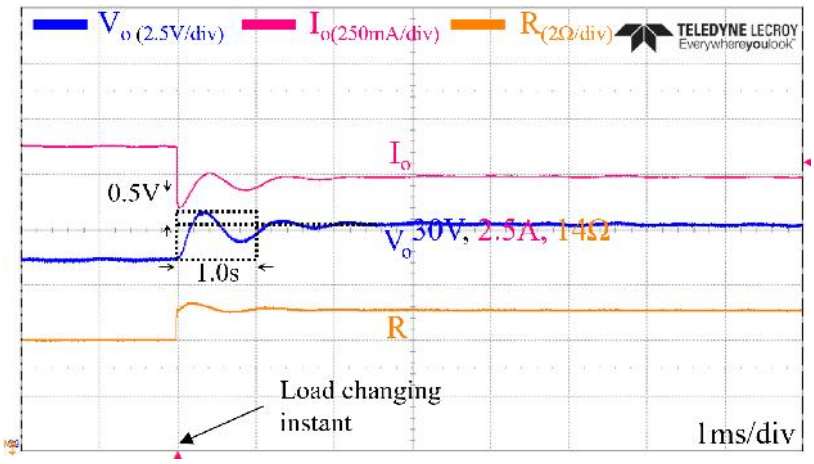


(c) 15Ω → 20Ω

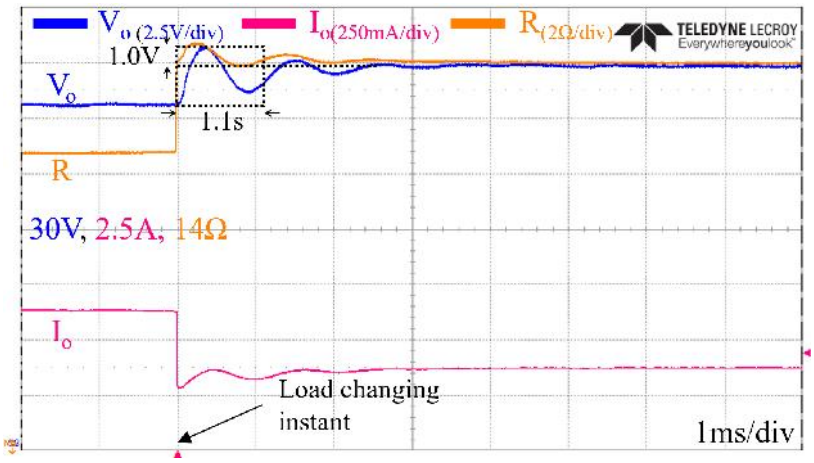
Figure 3-30: Hardware step load change of VS-CRC system



(a) 6.3Ω → 7Ω



(b) 10Ω → 11Ω



(c) 15Ω → 20Ω

Figure 3-31: Hardware step load change of RS-CRC system

Table 3.5: Hardware results

Operating point	Current segment		MPP		Voltage segment	
System	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)	Overshoot (V)	Settling time (ms)
CS-VRC	1.5*	oscillatory	1*	1.3	1.0*	0.8
RS-VRC	0*	0.8	0.5*	0.9	0.5*	0.8
VS-CRC	0.5	0.4	1.5	1.6	2.5	1.6
RS-CRC	0.5	0.4	0.5	1.0	1.0	1.1

$*^*$ = undershoot

In the CS-VRC system in Fig. 3-28, the undershoot becomes more significant for small load resistance, and the settling time is not constant. For the resistance of 7Ω, it shows under-damped oscillations. However, the RS-VRC system in Fig. 3-29 shows only a slight undershoot, and the settling time is almost constant. Therefore, it is proven that the current source segment is the worst-case for the CS-VRC systems, and the CS- VRC system shows load-dependent performance, but RS-VRC shows an almost constant dynamic response despite the load change.

CRC systems in Fig. 3-30 and Fig. 3-31 also show similar behavior as discussed in section IV.B. The experiment starts from a low resistance load (7Ω), showing the lowest overshoot and settling time, to a high load resistance (20Ω), showing increased overshoot and settling time. It shows that the RS-CRC system suppresses the performance degradation caused by the operating point shift. However, unlike the RS-VRC, RS-CRC is slightly sensitive to the operating point variation.

According to the experimental results, both simulation and experiment confirm all theoretical predictions for the four-control configurations.

3.6 Conclusion

According to the frequency domain and time domain analysis of this chapter, CS-VRC and VS-CRC systems are highly affected by reference generator gain and have an unstable root-locus, but RS-VRC and RS-CRC systems have a feature that reference generator dynamics are nullified. Thus, the resistance sensing method shows better performance, and the best performance is observed from the RS-VRC system. However, this nullification does not

happen when the load becomes CV or CC, although with the resistance sensing systems. In the simulation and experiment, the output behavior of the system coincides with the analysis of the model.

Chapter 4

Innovated control strategies for SAS

4.1 Overview

This section discusses the unified controller, fast reference generation technique, and SAS speed enhancement methods. In order to eliminate the control mode switching in hybrid control, a unified controller is presented by shifting the I-V curve by adding an offset voltage and current into the sensing signals according to the modified resistance reference generator. A small-signal model is tested by simulation and hardware.

Besides, the conventional Lambert-Ω function with explicit approximation form of PV equation is discussed. An approximated Lambert-Ω function is compared with conventional Lambert-Ω form and other iteration methods to verify the improvement of CPU cycle time consumption.

Moreover, the super-elliptic approximation for PV reference generation is tested for the SAS reference generator. Here, the accuracy of the model for a few commercial PV modules is compared with the conventional single diode model.

Finally, the limitation of the typical DC-DC converter is discussed, and the necessity of a bidirectional converter is demonstrated.

4.2 Unified controller for seamless operating range

The hybrid SAS controllers provide the maximum operating range, but its region-based operation makes some output voltage fluctuation when the control region change. Thus, the unified controller is demanded to provide at least the same operating range with single controller architecture.

4.2.1 Conventional hybrid control strategies

The hybrid SAS system concept provides a solution for such a limitation. In this case, VS-CRC and CS-VRC architectures are selectively activated according to the operating point location [6] as shown in Fig. 4-1a. Thus, this 2-section hybrid system provides uniform performance throughout VSS and CSS region of I-V curve but it degraded in the vicinity of MPP where the mode switching occurs.

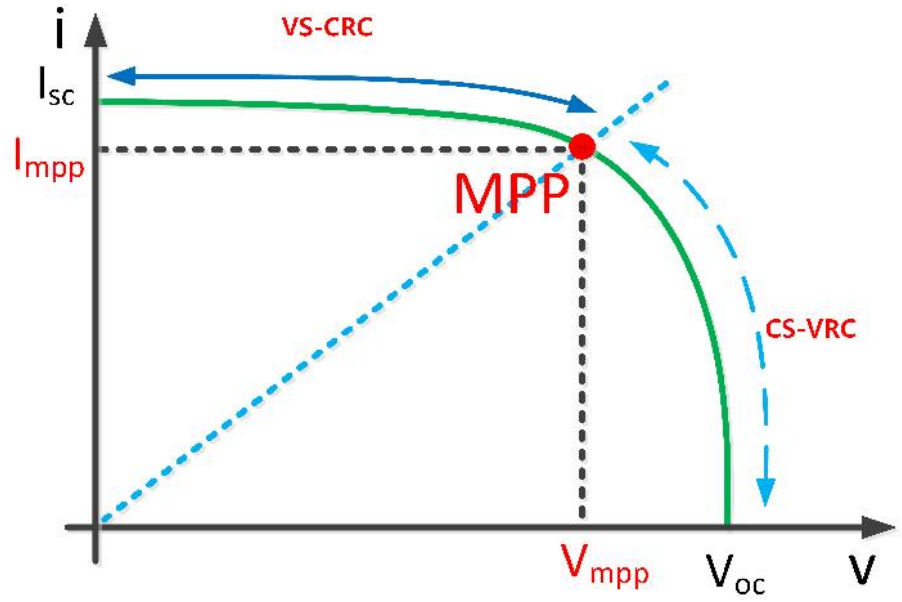
To maintain an equal performance on the entire I-V curve, a 3-section hybrid system as shown in Fig. 4-1b was implemented [7]. That provides an ideal solution for the enhancement of the SAS dynamic range. Here, resistance-based control [26, 91] is adapted for the vicinity of MPPT, and it can be a viable solution to lower the loop gain variation. The operating point defines resistance, and R-V characteristic curve can be plotted as Fig. 4-2. It reflects that a reference point can be generated depending on the resistance of the operating point.

Although the hybrid control enhances the SAS operating range, it generates another side effect in operation. Even the operating point moves between two control regions smoothly; it slightly fluctuates in the output due to switching the control loop. In section 4.2.4, the simulation and hardware experiment result of this issue is demonstrated.

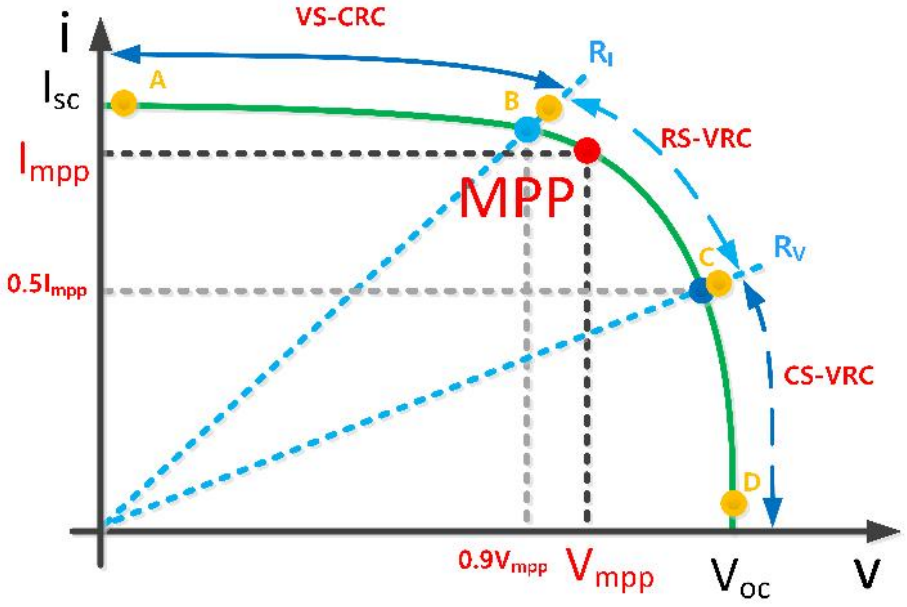
4.2.2 Proposed unified control strategy(MRS-VRC / MRS-CRC)

RS-based control shows the most stable SAS performance among the four SAS systems, as mentioned in Chapter-3. In this case, SAS output current is needed to be a non-zero value for numerical validity. According to the analysis of the PV system, the RS method is guaranteed the enhancement of the dynamic range. However, it also shows fluctuation near the I_{sc}. Unlike the voltage and current sensing system, the load resistance is always measured using the load current as the denominator in the resistance sensing system. The measured resistance usually becomes too large in the voltage source segment. That means near the open circuit condition, the resistance reaches an immense value (near infinity), and thus the k_{rv} and k_{iv} become so large that system stability can be lost.

Similarly, the I_{sc} condition is also critical because it needs to maintain a regulated current under deficient voltage conditions. In both V_{oc} and I_{sc} conditions, the converter duty cycle has become minimum according to the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation. In other words, they are the minimum power points of the PV curve, and power conversion should be close to zero. Such a condition



(a)



(b)

Figure 4-1: Segmentation of hybrid system (a) 2-section hybrid control [6] (b) 3-section hybrid control [7]

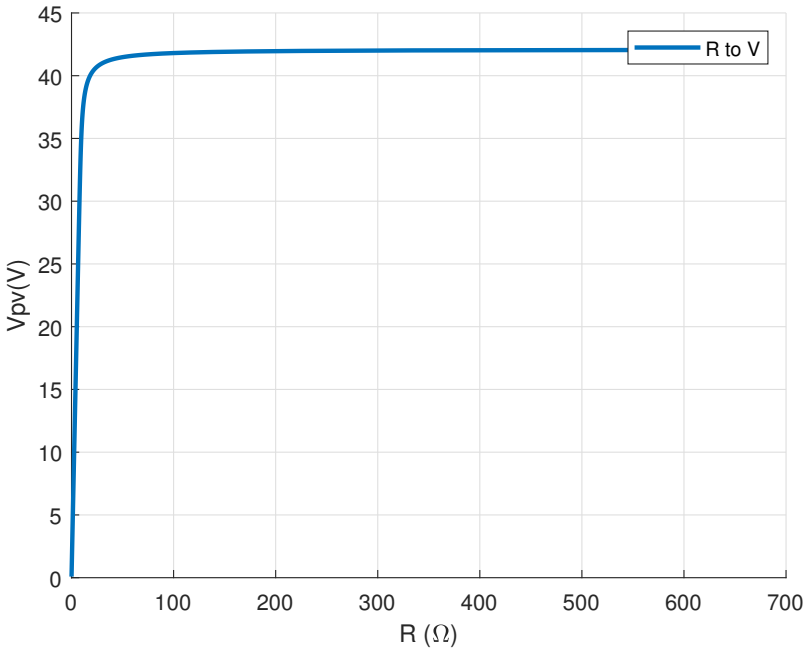


Figure 4-2: R to V reference generation curve

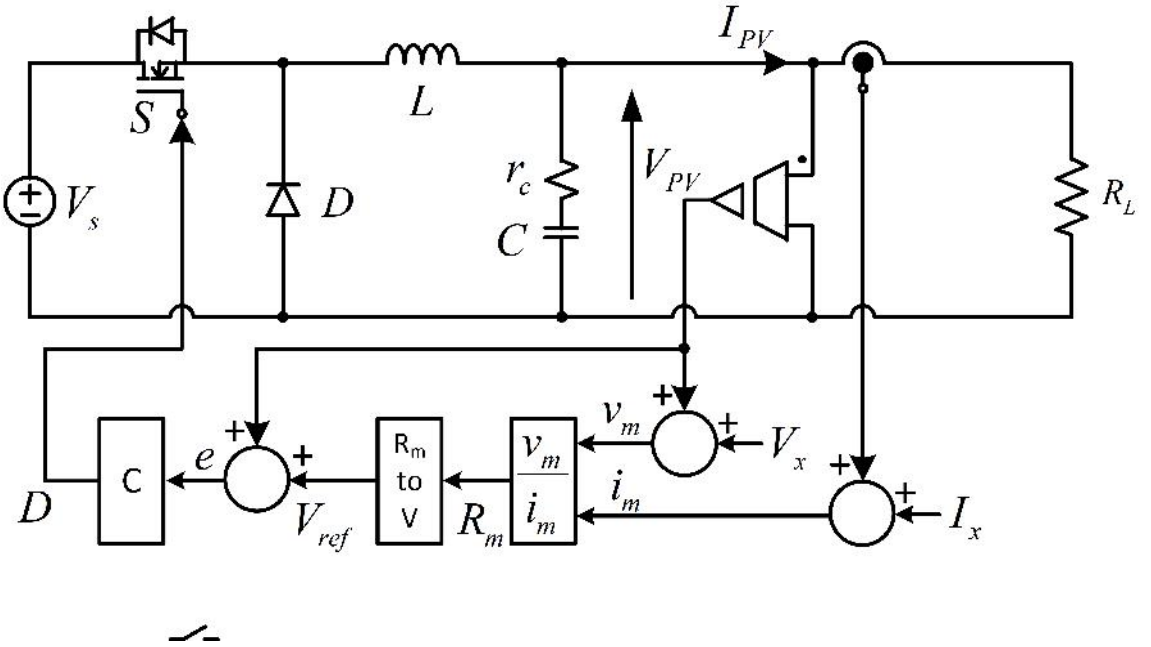
can easily cause instability in the system.

Our primary research objective is to develop a universal control scheme that extends the control range to the entire range of the I-V curve in a simple and numerically stable manner. Thus, our study mitigates this issue by shifting the origin point as Fig. 4-3. The formation of the modified resistance R_m is derived using (4.33).

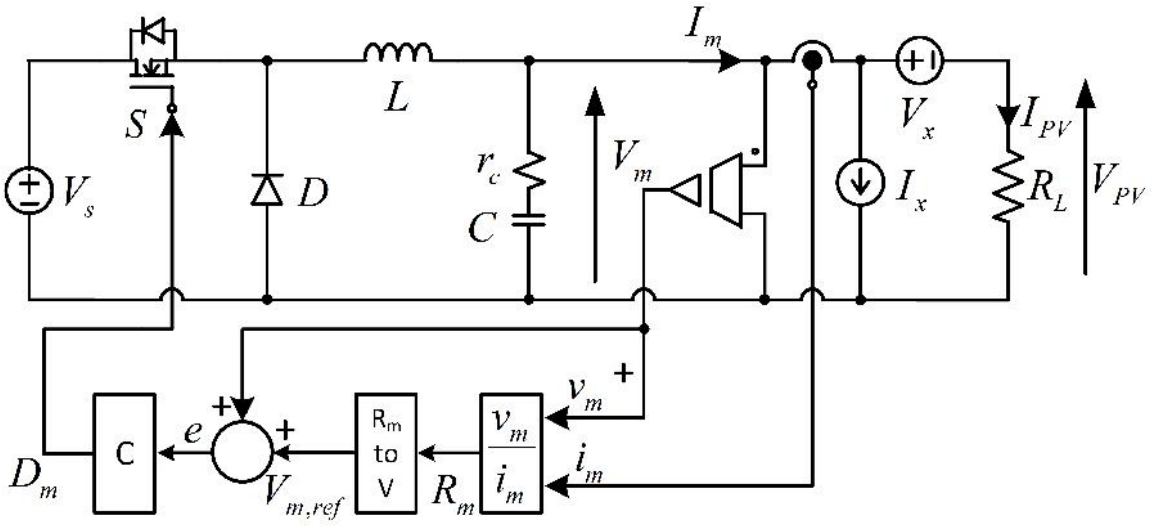
$$r_m = \frac{v + V_x}{i + I_x} = \frac{v_m}{i_m}. \tag{4.1}$$

Shifting the origin by V_x and I_x makes the feedback gain confined into a finite region that never becomes zero or infinity. There are two way to make this injection which named as soft injection and hard injection. In the soft injection, the V_x and I_x are add in to the voltage and current sensing signals of outer loop. Then, only the reference generation is processed with modified resistance and generate the reference. In the hard injection case, V_x and I_x are physically injected into output voltage and current then make the V_{opm} and I_m in the converter output. Thus, the reference become V_{opm} and I_m only the load voltage and current become V_{pv} and I_{pv}. Those two techniques guarantee appropriate outer feedback gain to have stable operation in the entire I-V curve.

According to this modification, the general super-elliptic curve can be consider as follows



(a)



(b)

Figure 4-3: Large signal model of (V_x, I_x)injection methods (a) Soft injection (b)Hard injection

[4,92].

$$\frac{(x-x_o)^n}{a^n}+\frac{(y-y_o)^n}{b^n}=1 \tag{4.2}$$

Thus, the approximated PV curve equation for the n=2 case can be modified as

$$\frac{(v-V_x)^2}{V_{oc}^2}+\frac{(i-I_x)^2}{I_{oc}^2}=1 \tag{4.3}$$

To realize the projection of origin, it can be described as shown in Fig. 4-4. In the case of soft injection, the output of the converter becomes V_{pv} and I_{pv}, thus the (V_x,I_x) origin is shifted into third quadrant as shown in Fig. 4-4a, but hard injection shifts the PV curve in positive direction on the first quadrant as shown in Fig. 4-4a.

In the hard injection, the V_{opm} and I_{opm} can be physically measured, but it is a virtual value in the soft injection. However, R_m generation is common for both circuits, and hard injection is used for stability analysis and simulation, and hardware is developed for the soft injection. According to that, the modified voltage, current, and resistance are defined in (4.4), (4.5), and (4.6) respectively. Here, note that $V_{opm}=V_{op}+V_x, I_{opm}=I_{op}+I_x$.

$$v_{opm}=V_{oc}\sqrt{1-\left(\frac{i_{opm}-I_x}{I_{sc}}\right)^2}+V_x \tag{4.4}$$

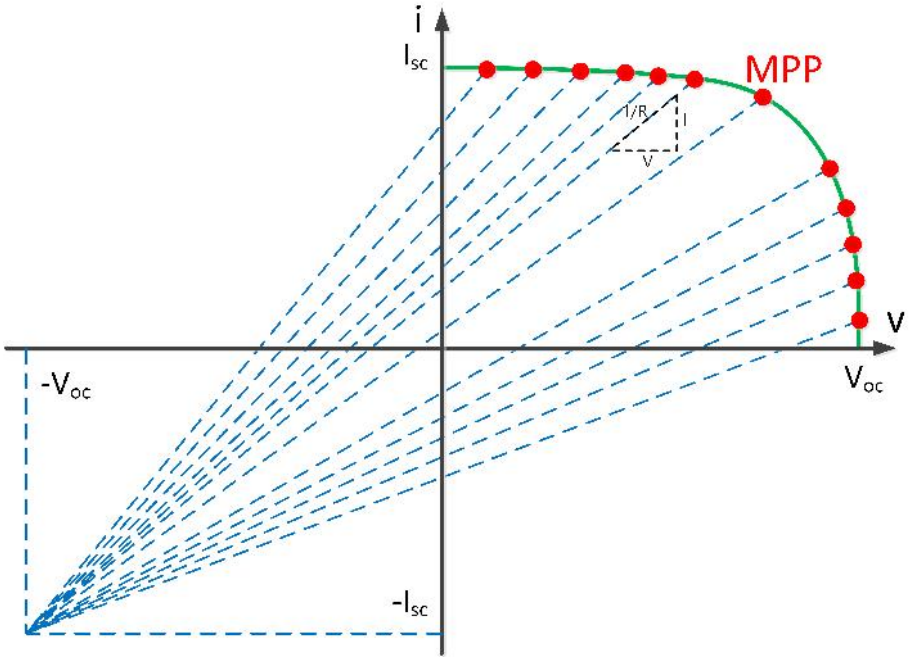
$$i_{opm}=I_{sc}\sqrt{1-\left(\frac{v_{opm}-V_x}{V_{oc}}\right)^2}+I_x \tag{4.5}$$

$$r_m=\frac{v_{opm}}{I_{sc}\sqrt{1-\left(\frac{v_{opm}-V_x}{V_{oc}}\right)^2}+I_x} \tag{4.6}$$

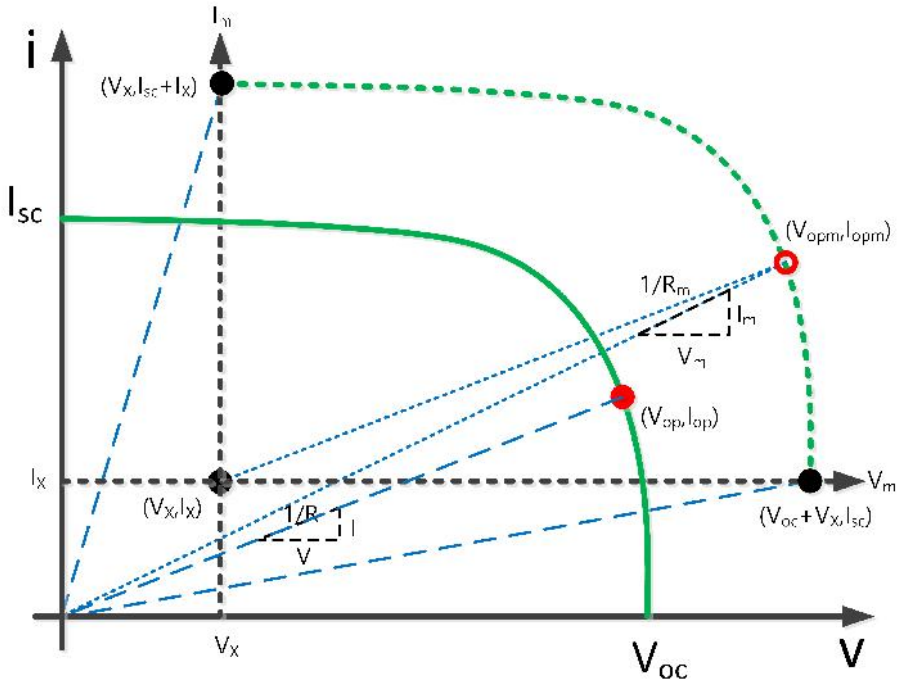
When substitute the $V_{opm}=V_{op}+V_x$,

$$r_m=\frac{V_{op}+V_x}{I_{sc}\sqrt{1-\left(\frac{v_{op}}{V_{oc}}\right)^2}+I_x} \tag{4.7}$$

The behavior of R_m according to the (V_x,I_x) shown in Fig. 4-5. It explains all behaviors of r_m. When the V_x goes infinity,r_m also goes infinity, which is needed to avoid in the RS method. Thus, the best value for the V_x becomes zero, but due to the advantages of the V_x, it is better to limit maximally around V_{ocn}, which makes the r_m double. Contrary, I_x shows the opposite behavior in which the r_m becomes infinity when I_x goes to zero. However, larger I_x makes the low resolution of r_m; thus, it is better to limit the I_x maximally around



(a)



(b)

Figure 4-4: Reference generation of MRS method (a) Soft injection (b)Hard injection

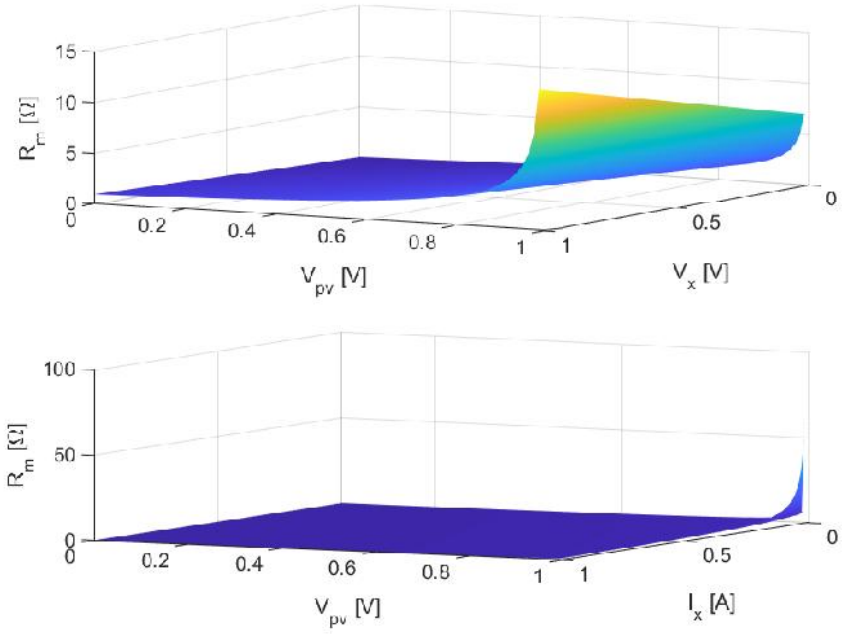


Figure 4-5: Behavior of R_m according to the individual V_x and I_x variation

I_{scn}, which makes the convergence of $r_m I_x$.

Now, the values for the (V_x,I_x) can be defined according to the injection method. First, the soft injection method can be considered. By considering both graph in 4-5 together, R_m according to both (V_x,I_x) in PSIM simulation can be plotted as shown in Fig. 4-6. Here, the non-linearity of R_m is reduced when the (V_x,I_x) is increased but the difference is reduced. The gradient of R_m on the V_{oc} can be taken for the comparison, because the curve slopes are monotonically increased and maximum on V_{oc}. The values are noted in Table 4.1. It shows that gradient become slightly change when the (V_x,I_x) increases than (V_{oc},I_{sc}) values. Thus, ($-V_{oc}$,$-I_{sc}$) point can be consider as the maximum point of the (V_x,I_x). The minimum points can be determined according to the noise magnitude of the CS and VS signals to avoid the sensing values become zero.

The (V_x,I_x) range of the hard injection is quite limited than the soft injection method. The hard injection can increase the operating range of the SAS by two aspects. As a first way, I_x can be used to eliminate the DCM operation of the converter. Because CCM guarantees the small voltage ripple of the power converter, but DCM, which happens in the small output current condition, makes considerable ripple magnitude, and thus, SAS performance will deteriorate as well as MPPT operation of PCS connected to the SAS. Thus, it is required to maintain a minimum dummy current to keep the CCM operation.

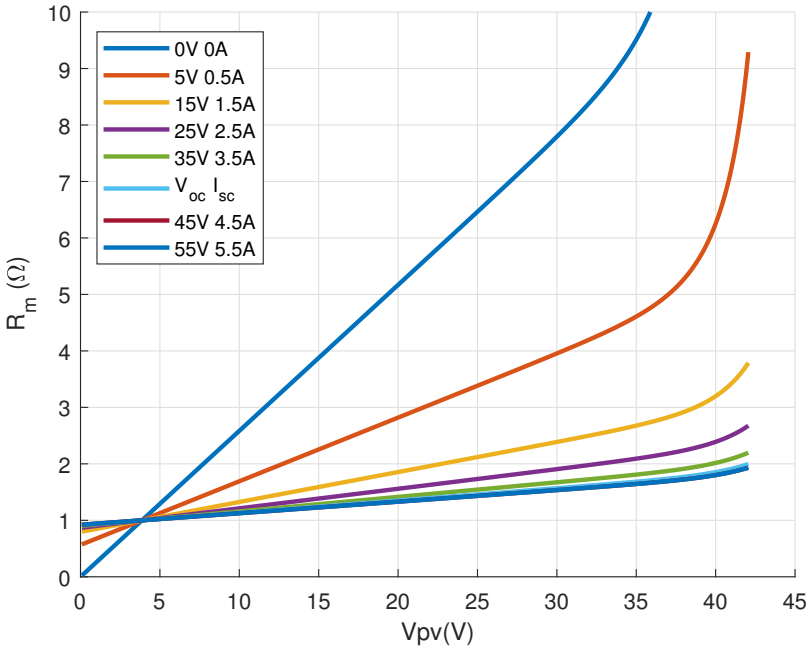


Figure 4-6: The R_m according to the simultaneous changing of (V_x,I_x) values

Table 4.1: R_m and maximum gradient on V_{oc} under different (V_x,I_x) values

(V_x,I_x)	R_m (Ω)	Gradient of R_m (Ω/V)
0V,0A	∞	∞
5V,0.5A	9.29	220.67
15V,1.5A	3.79	89.96
25V,2.5A	2.67	63.55
35V,3.5A	2.20	52.20
V_{oc},I_{sc}	2.00	47.41
45V,4.5A	1.93	45.89
55V,5.5A	1.93	45.89

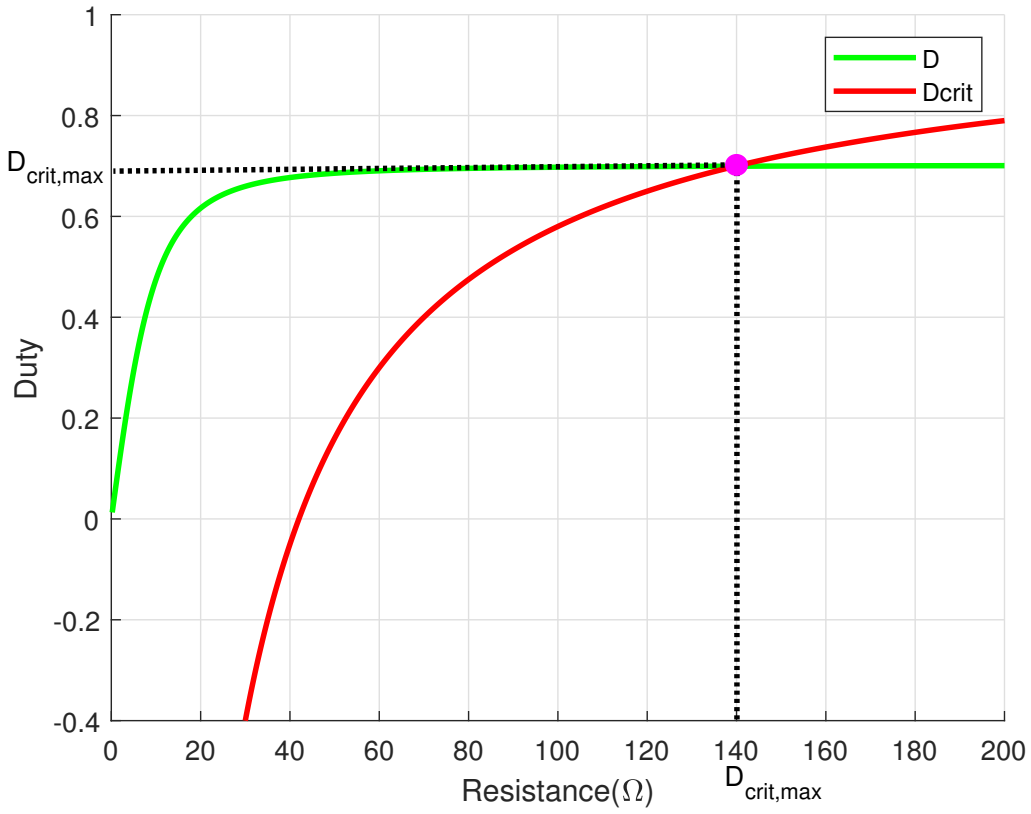


Figure 4-7: Behavior of SAS duty and critical duty of CCM boundary condition vs load resistance

Naturally, SAS system load is not fixed, and duty changes according to the operating point variation. Thus, critical resistance (R_{crit}) cannot be directly defined. Instead, a function of critical duty ratio can be obtained as a function of load resistance as

$$D_{crit} = 1 - \frac{2L}{R_L T_s}. \tag{4.8}$$

The duty cycle of the SAS system under CCM conditions can be derived by equations of approximated PV curve and buck converter duty equation. Then the duty vs. load resistance becomes

$$D = \frac{1}{V_s \sqrt{\left(\frac{1}{R_L I_{sc}}\right)^2 + \left(\frac{1}{V_{oc}}\right)^2}}. \tag{4.9}$$

The intersection of (4.8) and (4.9) is shown in Fig. 4-7, and that critical duty can be considered the boundary of the CCM. It reflects that $D > D_{CRIT}$ SAS is operating under CCM and intersection point can be named D_{CRIT}. In this case, D_{CRIT} becomes 0.7 under

140Ω, and if the resistance increases further, the converter enters DCM operation. Then the voltage under D_{CRIT} becomes

$$V_{CRIT} = V_s D_{CRIT} = 42V \tag{4.10}$$

The current of that operating point becomes

$$I_{CRIT} = \frac{V_{CRIT}}{R_{CRIT}} = 300mA \tag{4.11}$$

This current can be taken as the injecting current magnitude (I_x) of the unified controller.

In the case of short circuit operation points, SAS should provide the minimum duty ratio to maintain an extremely low output voltage. To achieve the zero-output voltage, the minimum on-time of gate driver and MOSFET make a limitation. As the second way, V_x can avoid this minimum output voltage affection to the load.

The slew rate of the gating channel is the origin of minimum on-time limitation, and that information is available on the component datasheet. A detailed description of the minimum one-time limitation for the buck converter can be found in [93], and recommended minimum on-time t_{min} can be justified as

$$t_{min} = 0.4 t_{on\_min} \tag{4.12}$$

where t_{on_min} is the calculated minimum duty cycle. In this experiment setup, the UCC21222 gate diver has 10ns minimum on time but, the IRF740 MOSFET generates the largest delay time. The t_{on_min} can be calculated as

$$t_{on\_min} = t_{d(on)} + t_r + t_{d(off)} + t_f + t_{rr} \tag{4.13}$$

where, $t_{d(on)}$ is the turn-on delay time, t_r is the rise time, $t_{d(off)}$ is the turn-off delay time, t_f is the fall time, and t_{rr} is the body diode reverse recovery time. Thus, effective t_{min} becomes 1.267μs. 100kHz f_{sw} makes cycle time t_s 10μ, and it determines the D_{min} as follows

$$D_{min} = t_{min}/t_s = 0.127V \tag{4.14}$$

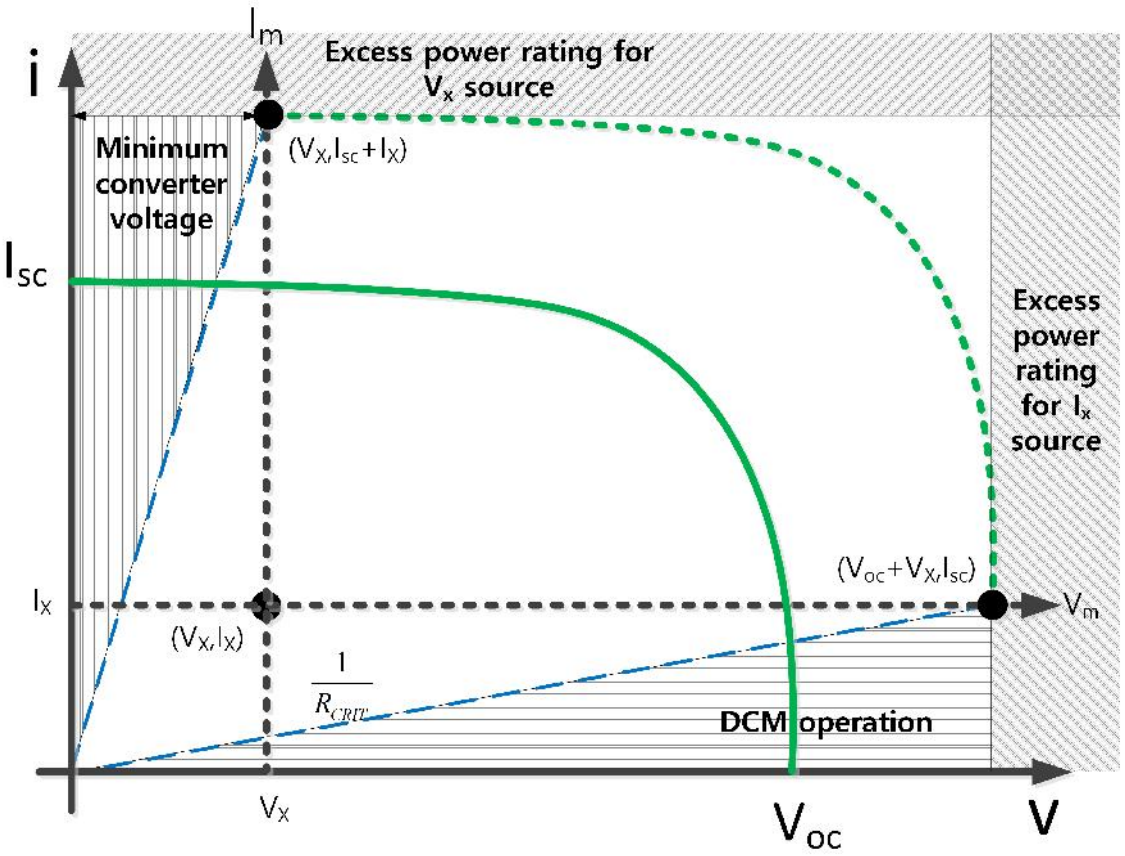


Figure 4-8: Operating conditions of unified controller under hard injection

Then, the achievable minimum output voltage can be calculated as

$$V_{o,min} = D_{min} \times V_s = 7.6V \tag{4.15}$$

This $V_{o,min}$ can be used as the injecting voltage magnitude (V_x) of the unified controller.

To minimize the power consumption of the (V_x) and (I_x) source, it needs to be limited to $V_{o,min}$ and I_{CRIT}, respectively. The working area of hard injection can be identified as shown in Fig. 4-8

As an implementation of the experimental setup, those voltage and current sources can be set up using active loads according to Fig. 4-3a. This implementation will be completed in future works.

4.2.3 Modeling of the unified controller

4.2.3.1 Reference generator

To obtain the reference from the modified resistance, (4.1) is substituted into (4.4) or (4.5). Then, the reference signal in MRS-VRC becomes

$$v_{mref} = \frac{V_x I_{sc}^2 + \frac{I_x}{r_m} V_{oc}^2 + \sqrt{(V_x I_{sc}^2 + \frac{I_x}{r_m} V_{oc}^2)^2 - (I_{sc}^2 + \frac{V_{oc}^2}{r_m^2})(V_x^2 I_{sc}^2 + I_x^2 V_{oc}^2 - V_{oc}^2 I_{sc}^2)}}{I_{sc}^2 + \frac{V_{oc}^2}{r_m^2}} \quad (4.16)$$

and the reference signal of MRS-CRC becomes

$$i_{mref} = \frac{r_m V_x I_{sc}^2 + I_x V_{oc}^2 + \sqrt{(r_m V_x I_{sc}^2 + I_x V_{oc}^2)^2 - (r_m^2 I_{sc}^2 + V_{oc}^2)(V_x^2 I_{sc}^2 + I_x^2 V_{oc}^2 - V_{oc}^2 I_{sc}^2)}}{r_m^2 I_{sc}^2 + V_{oc}^2}. \quad (4.17)$$

Here, r_m is the resistance calculated by modified output voltage and current in (4.1). Numerically, the 4.16 and 4.17 have negative roots but it can be neglect, because only the first quadrant of the super-ellipse is considered as PV model equation.

According to (4.1), small-signal model describing the first step is given by

$$\hat{r_m} = k_{r_m v}\hat{v} + k_{r_m i}\hat{i} \quad (4.18)$$

where the two small-signal gains at the operating point are given respectively by differential gains,

$$k_{r_m v} = \frac{\hat{r_m}}{\hat{v}}\Big|_{(V_{opm}, I_{opm})} = \frac{1}{I_{op} + I_x}, k_{r_m i} = \frac{\hat{r_m}}{\hat{i}}\Big|_{(V_{opm}, I_{opm})} = -\frac{V_{op} + V_x}{(I_{op} + I_x)^2} \quad (4.19)$$

Meanwhile, the small-signal model describing the second step is given in two cases. If a reference is given by $v_{mref} = f(r_m)$ as in (10), the small-signal gain at the operating point (V_{opm}, I_{opm}) is given as follows:

$$k_{v_{mref}, r_m} = \frac{\hat{v_{mref}}}{\hat{r_m}}\Big|_{(V_{opm}, I_{opm})} \quad (4.20)$$

Similarly, when the reference has the form as $i_{mref} = g(r_m)$ as in (11), the small-signal gain is given by

$$k_{i_{mref}, r_m} = \frac{\hat{i_{mref}}}{\hat{r_m}}\Big|_{(V_{opm}, I_{opm})}. \quad (4.21)$$

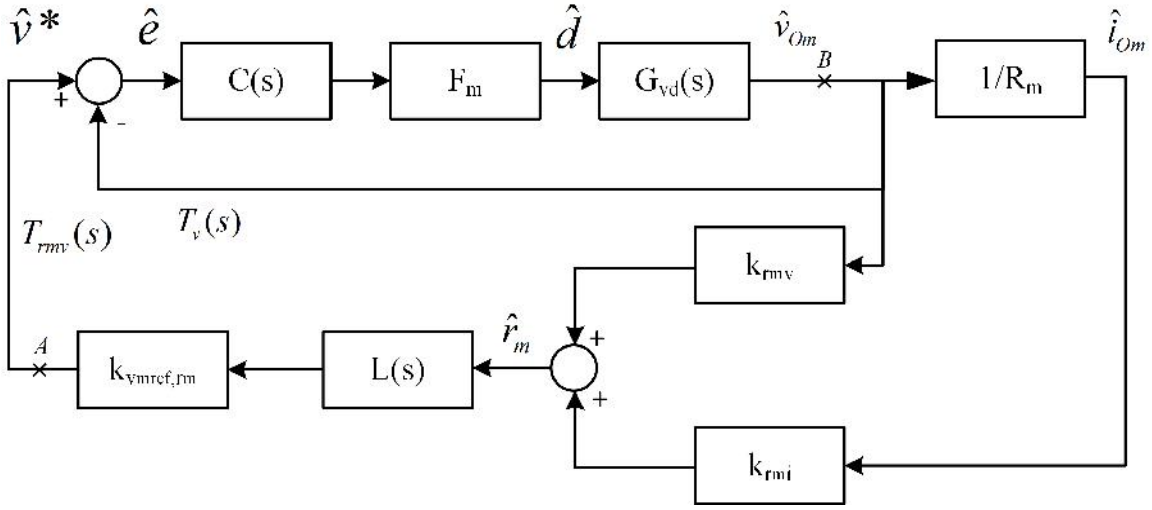


Figure 4-9: Small-signal block diagram of MRS-VRC system

4.2.3.2 MRS-VRC

The MRS-VRC configuration can be modeled as shown in Fig. 4-9, and reference loop gain is given as follows.

$$T_v(s) = F_m C(s) G_{vd}(s) \tag{4.22}$$

and

$$T_{rmv}(s) = F_m C(s) G_{vd}(s) k_{v_{ref},r_m} \left(k_{r_m v} + \frac{k_{r_m i}}{R_m} \right) L(s) \tag{4.23}$$

Thus, the overall loop gain becomes

$$T_B(s) = F_m C(s) G_{vd}(s) K_5(s) \tag{4.24}$$

where

$$K_5(s) = 1 - k_{v_{ref},r_m} \left(k_{r_m v} + \frac{k_{r_m i}}{R_m} \right) L(s) \tag{4.25}$$

and k_{v_{ref},r_m} is the small-signal gain according to the curve slope of the solar module.

Since the following condition is always met:

$$k_{r_m v} + \frac{k_{r_m i}}{R_m} = \frac{1}{I_{op} + I_x} - \frac{(V_{op} + V_x)/(I_{op} + I_x)^2}{(V_{op} + V_x)/(I_{op} + I_x)} = 0, \tag{4.26}$$

by substituting (4.26) into (4.25), we get $K_5(s) \equiv 1$. This observation shows how the modified resistance-sensing reference generation structure also can eliminate the effects of inter-loop interactions similar to the RS-VRC system. The Fig.4-10a also reflects that the

bode plot of the MRS-VRC system are independent of the operating point under CV load.

4.2.3.3 MRS-CRC

Also, the MRS-CRC configuration can be modeled as shown in Fig. 4-11, and reference loop gain is given as follows.

$$T_B(s) = T_i(s) + T_{rmi}(s) \tag{4.27}$$

where the loop gains of the MRS-CRC structure can be written as

$$T_i(s) = F_m C(s) G_{iod}(s) \tag{4.28}$$

and

$$T_{rmi}(s) = F_m C(s) G_{iod}(s) L(s) k_{i_{mref},r_m} \left(k_{r_mi} + k_{r_mv} R_m\right) \tag{4.29}$$

Accordingly, the overall loop gain becomes

$$T_B(s) = F_m C(s) G_{iod}(s) K_6(s) \tag{4.30}$$

where

$$K_6(s) = 1 - k_{i_{mref},r_m} \left(k_{r_mi} + k_{r_mv} R_m\right). \tag{4.31}$$

Similarly to the MRS-CRC system, $K_6(s)$ is unity since

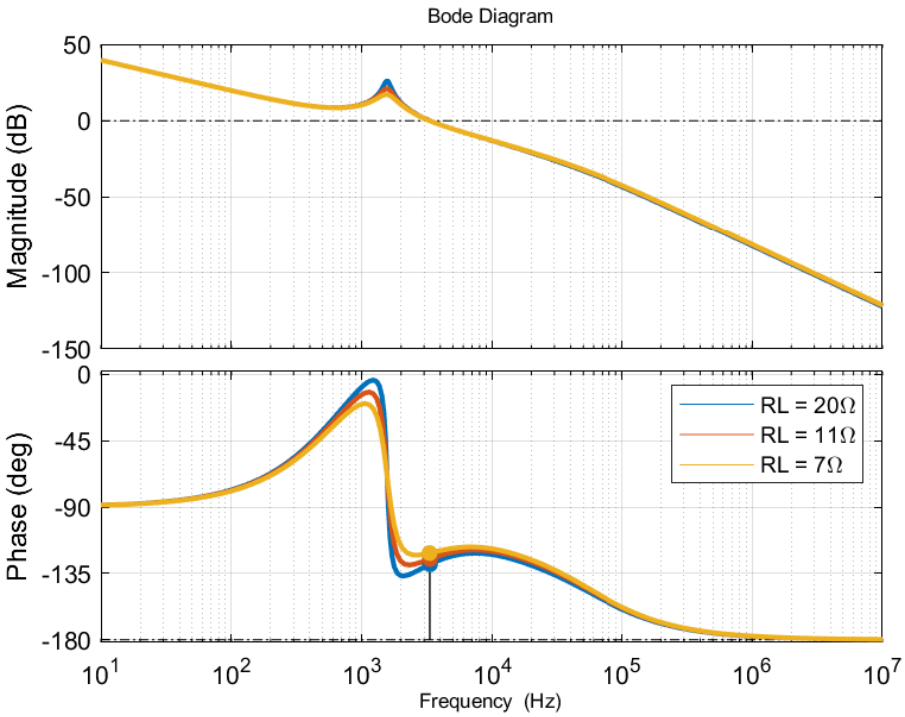
$$k_{r_mi} + k_{r_mv} R_m = -\frac{V_{op} + V_x}{(I_{op} + I_x)^2} + \frac{1}{(I_{op} + I_x)} \frac{V_{op} + V_x}{(I_{op} + I_x)} = 0. \tag{4.32}$$

This result reflects the ability of the MRS-CRC system again also maintain stability conditions of the RS-CRC system. The Fig.4-10a also reflects that the bode plot of the MRS-CRC system are independent of the operating point under CV load.

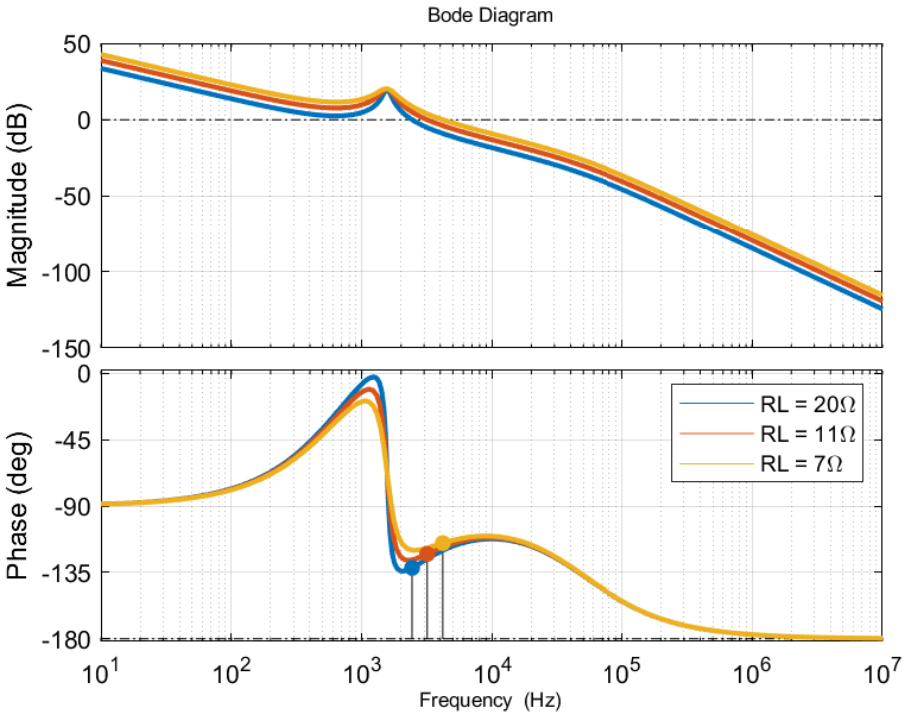
4.2.4 Comparison of hybrid and unified controller

This approach aims to develop an integrated control method that extends the control range to the full range of the I-V characteristic curve in a simple and numerically stable manner. For this study, the proposed modified resistance R_m is taken as (4.33) .

$$R_m = \frac{v + V_{ocn}}{i + I_{scn}}. \tag{4.33}$$



(a)



(b)

Figure 4-10: Bode diagrams of the unified controller overall loop gain (a) MRS-VRC (b) MRS-CRC

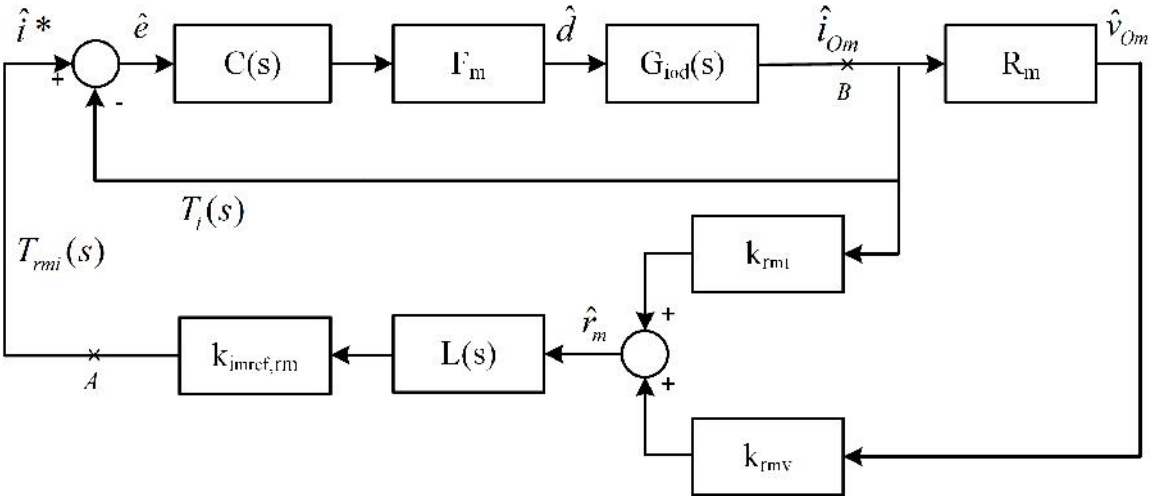


Figure 4-11: Small-signal block diagram of MRS-CRC system

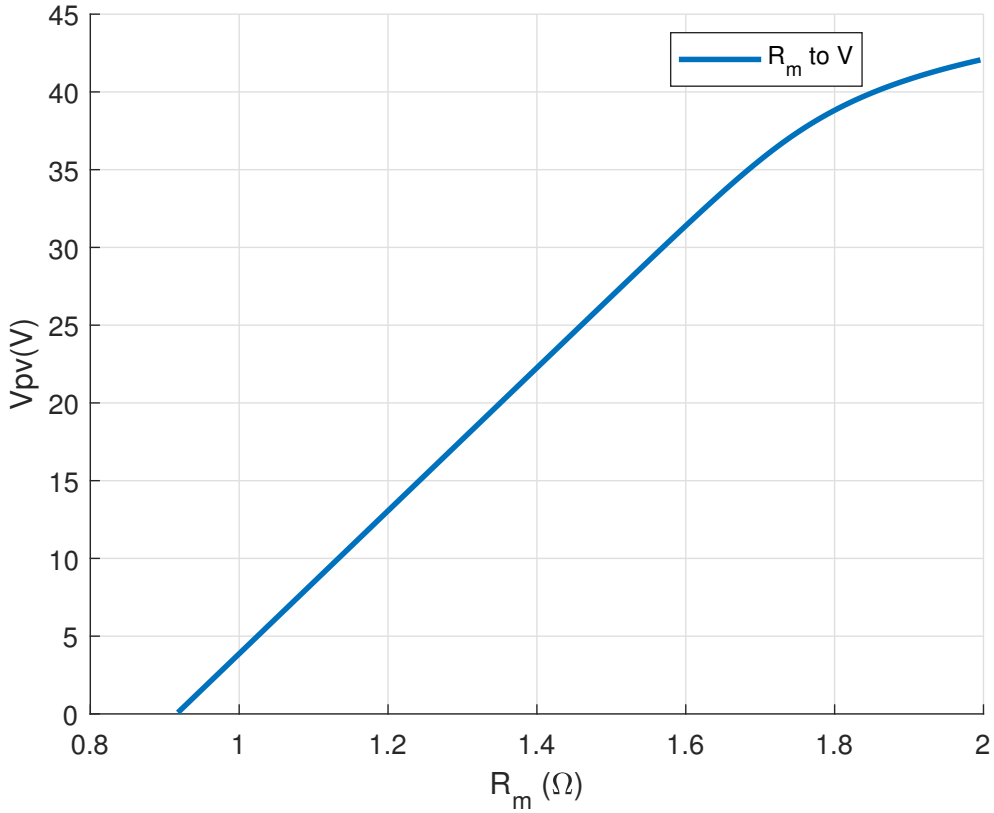


Figure 4-12: Rm-V characteristic curve

In this study, the V_x and I_x are set to V_{ocn} and I_{ocn}, respectively. According to the changed resistance definition, the outer loop is limited to a finite value from $R_{m,min}$ to $R_{m,max}$

$$R_{m,min} = \frac{V_{ocn}}{2I_{scn}} \tag{4.34}$$

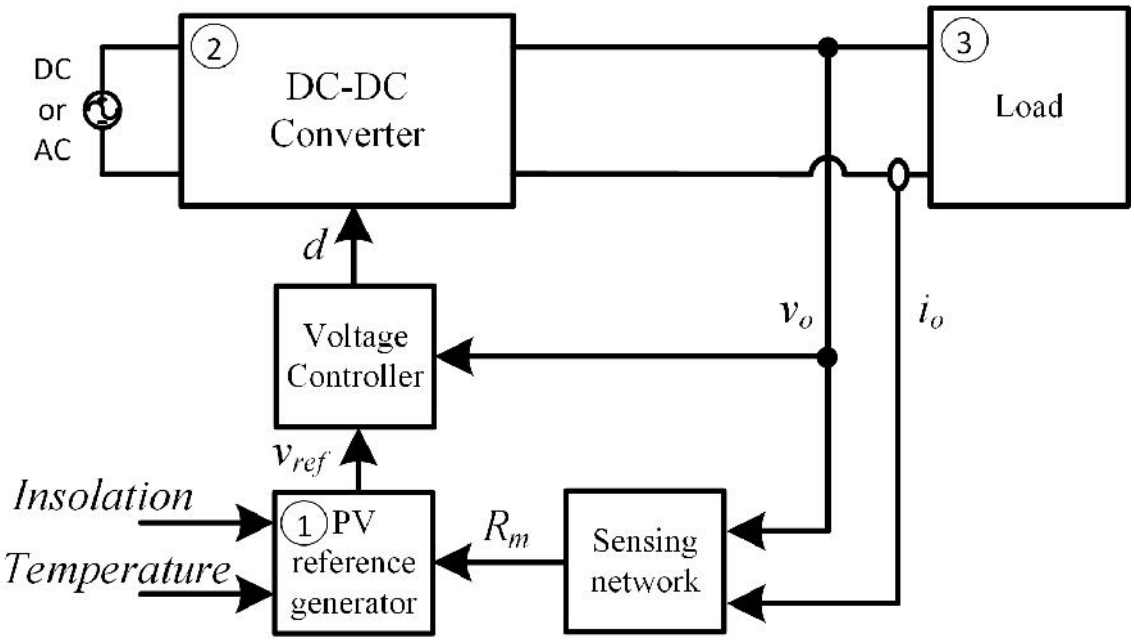


Figure 4-13: Block diagram of modified resistance system

and

$$R_{m,max} = \frac{2V_{ocn}}{I_{scn}}, \tag{4.35}$$

ensuring numerical stability in the control loop. Therefore, in the proposed control method, the reference is generated using the $R_m - V$ conversion. The reference voltage is determined according to R_m as shown in Fig. 4-12 and Fig. 4-13 shows the system block diagram. By using G_{vd} and G_{i_od} in Chapter-2.3, the desired controller parameters in (4.36) were designed as in Table 4.2 and 4.3.

$$C[z] = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + +a_2 z^{-2}}. \tag{4.36}$$

The hybrid and unified systems were implemented on PSIM under different load variations to verify the result, as shown in 4-3a. Different kinds of load tests can proceed as a combination of various control loop regions. In this research, the voltage region to MPP region is preferred and used, limiting step load variation under the three operating points in each control loop region were tested. Experimental results for the load resistances ranging from 40Ω to 12Ω are shown in Fig. 4-14 for the unified controller. Table 4.4 depicts the observed changes in parameters under these conditions. Also, the dynamic load changing performance was tested by sweeping the output resistance. In this case, the CSS to MPP region was used, and output voltage and duty cycle were plotted under the insolation of

Table 4.2: Parameters of hybrid controller

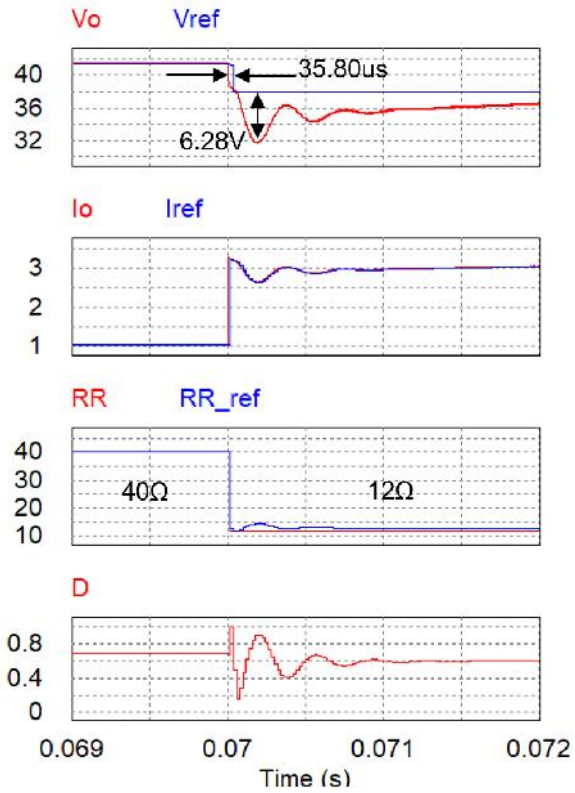
Controller		Parameter
Sampling frequency		50kHz
Current Mode	k_p	0.17271
	k_i	2302.8
	Cutoff frequency	19.7kHz
RS-VRC	k_p	0.1259642
	k_i	292.94
	Cutoff frequency	6kHz
CS-VRC	b_0	0.291435
	b_1	-0.08753
	b_2	0.158257
	a_1	0
	a_2	-1
	Cutoff frequency	18.0kHz

Table 4.3: Parameters of unified controller

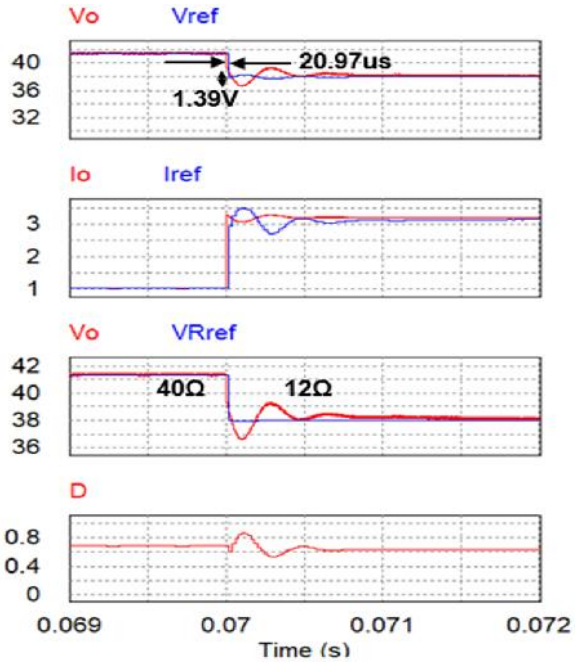
Controller		Parameter
Sampling frequenc		50kHz
Voltage Mode	Phase margin	64.6°
	Gain margin	-343dB
	Cutoff frequency	3.98kH
	Settling time	$759\mu s$
	b_0	0.3136972
	b_1	-0.49367104
	b_2	0.18500096
	a_1	-1
	a_2	0

Table 4.4: Simulation results

System	Reference switching delay (μs)
Hybrid system	35.80
Unified system	20.97



(a)



(b)

Figure 4-14: Comparison of step load change (a)Hybrid controller with 3-section (b)Unified controller (MRS-VRC)

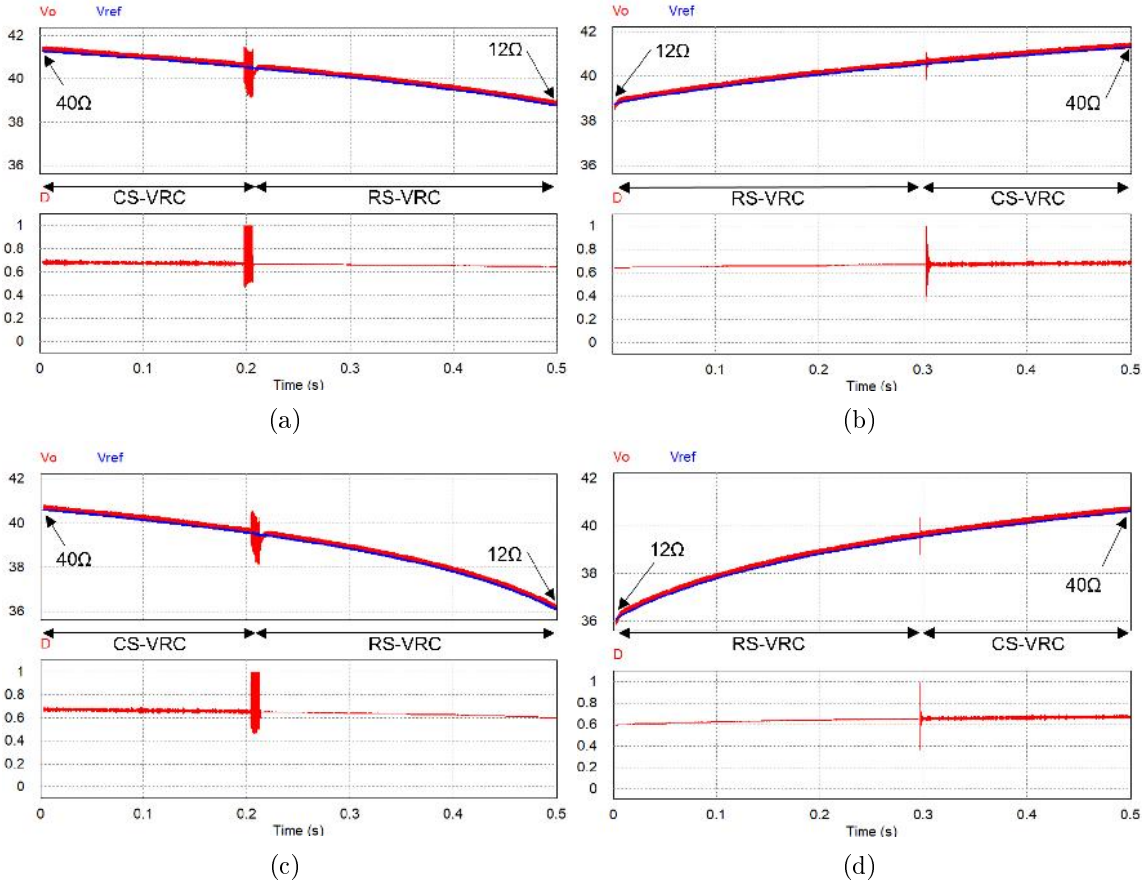


Figure 4-15: Simulation results (25°C, linear load change $R_L = 40\Omega \leftrightarrow 12\Omega$) of the hybrid controller (a)$1000W/m^2$ load decrement (b)$1000W/m^2$ load increment (c) $800W/m^2$ load decrement (d)$800W/m^2$ load increment

$1000W/m^2$ and $800W/m^2$ as shown in Fig. 4-15 and Fig. 4-16, respectively.

According to the load step change in Fig. 4-14 and Table 4.4, the unified controller required less transient time than the hybrid system due to the removal of control mode switching. The mode switching in hybrid control caused the larger undershoot because the control variables must be refreshed after changing the controller. During this period, duty reaches the maximum limit and is clamped to the limit value. Fig. 4-14b shows that the unified controller has a less settling time and unsaturated duty cycle.

The dynamic response of both SAS systems was observed, as shown in Figs. 4-15 and 4-16. In the case of the hybrid system, the output voltage has a fluctuation when the controller is switched. For the MPPT operation, such a slight voltage fluctuation is also realized, which reduces the MPPT performance. Especially in the GMPPT, the operating point is switched rapidly, and MPP can be located near the CSS and VSS region boundary. In such a case, the hybrid system may disturb the MPPT operation.

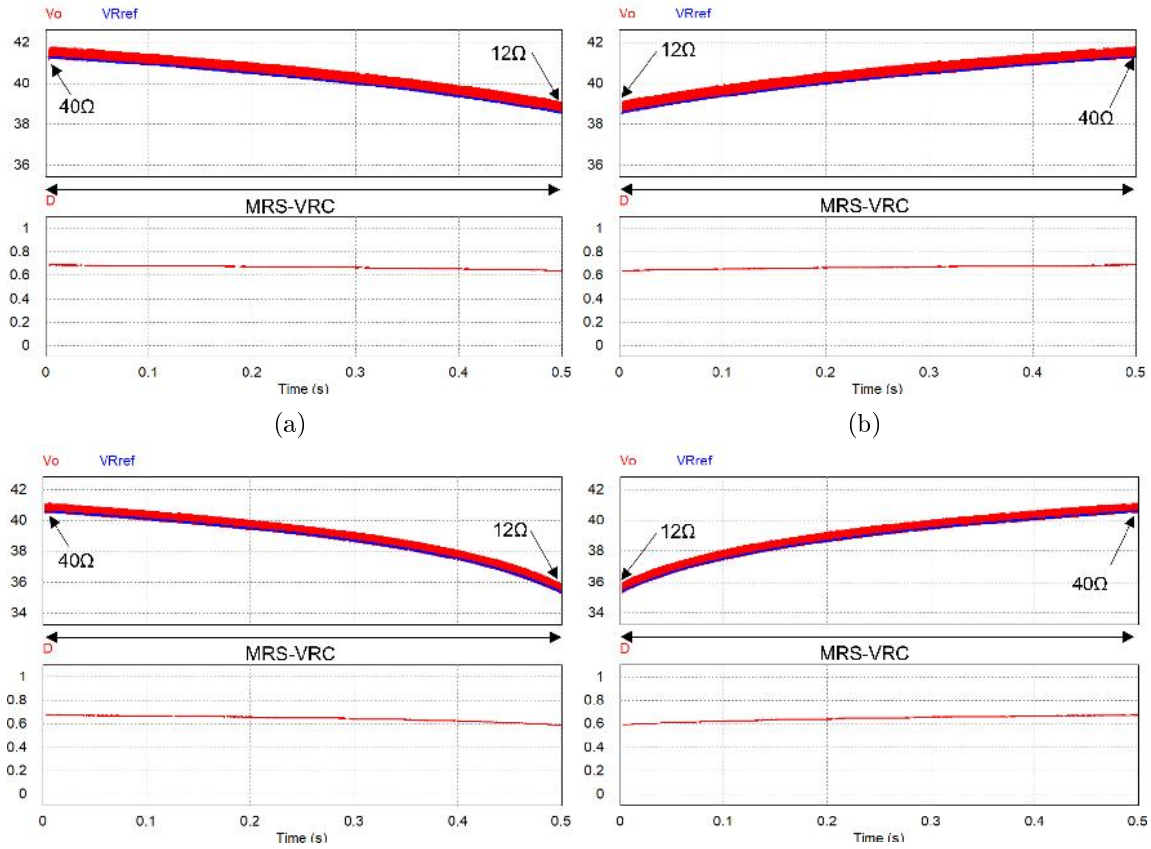


Figure 4-16: Simulation results (25°C, linear load change $R_L = 40\Omega \leftrightarrow 12\Omega$) of the unified controller (a)$1000W/m^2$ load decrement (b)$1000W/m^2$ load increment (c) $800W/m^2$ load decrement (d)$800W/m^2$ load increment

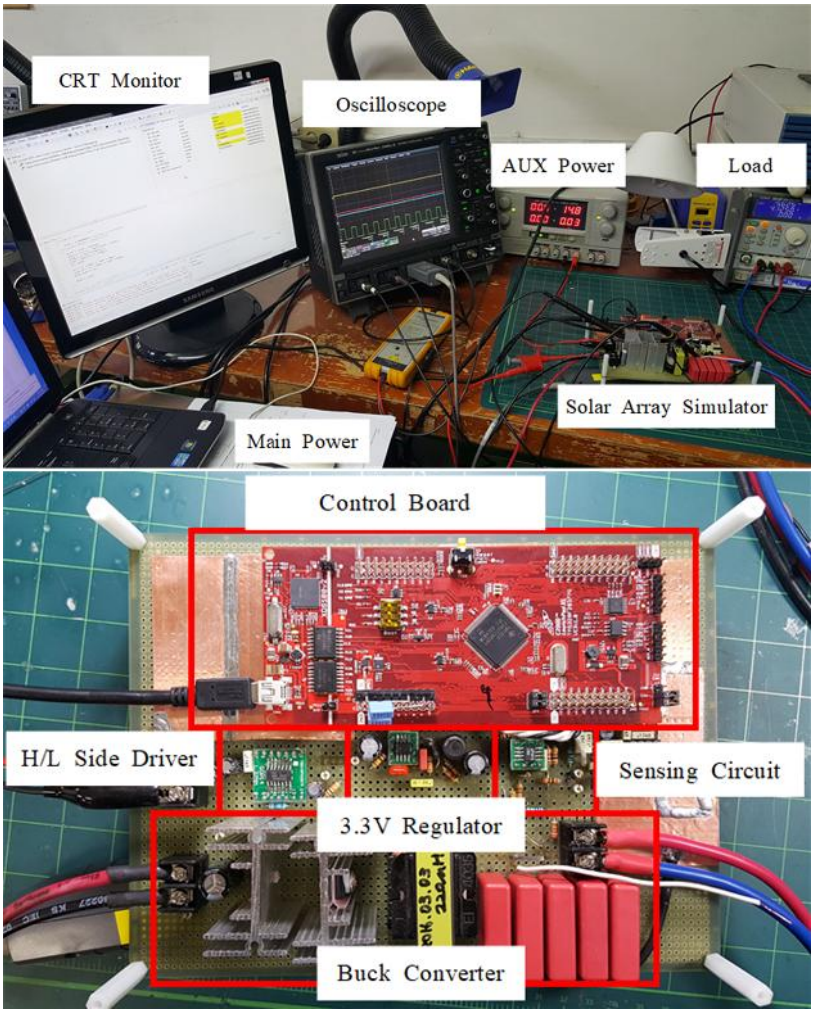
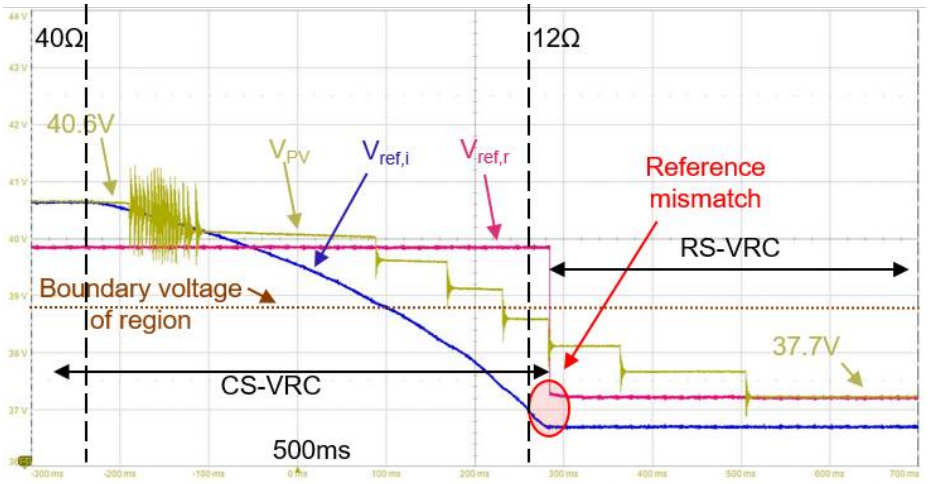
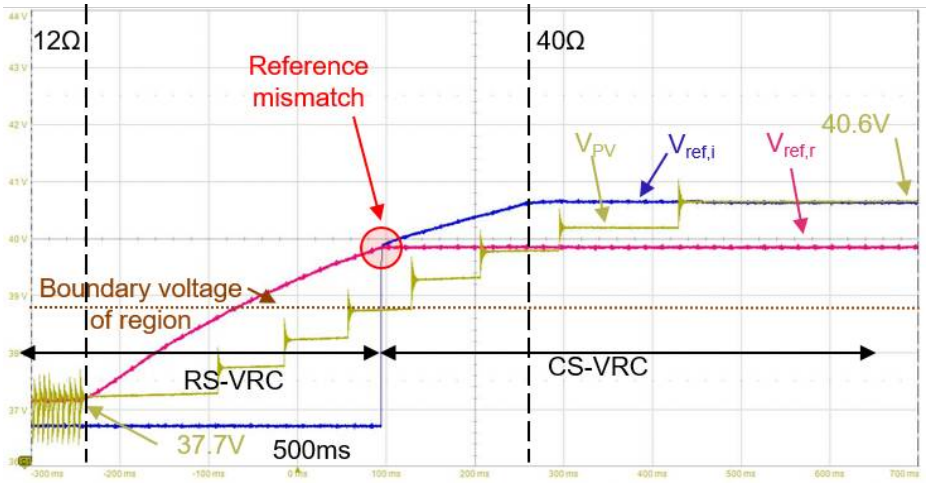


Figure 4-17: Hardware setup for the performance comparison



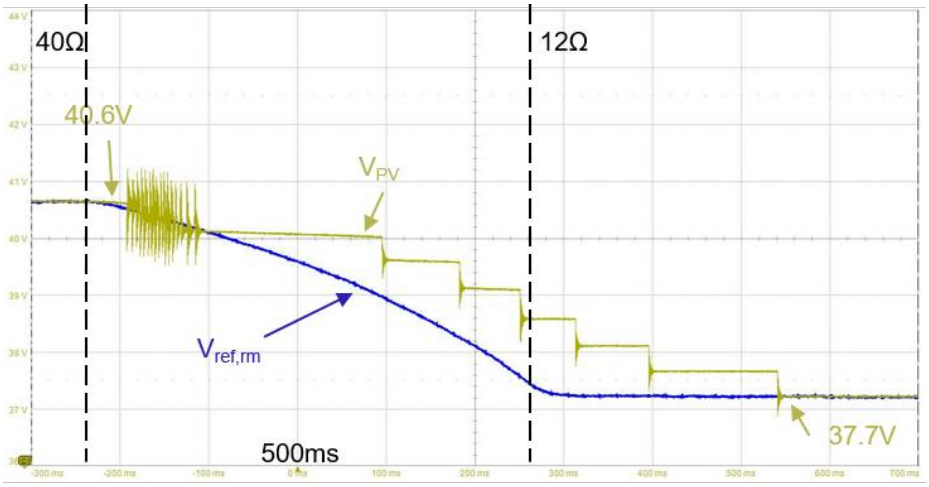
(a)



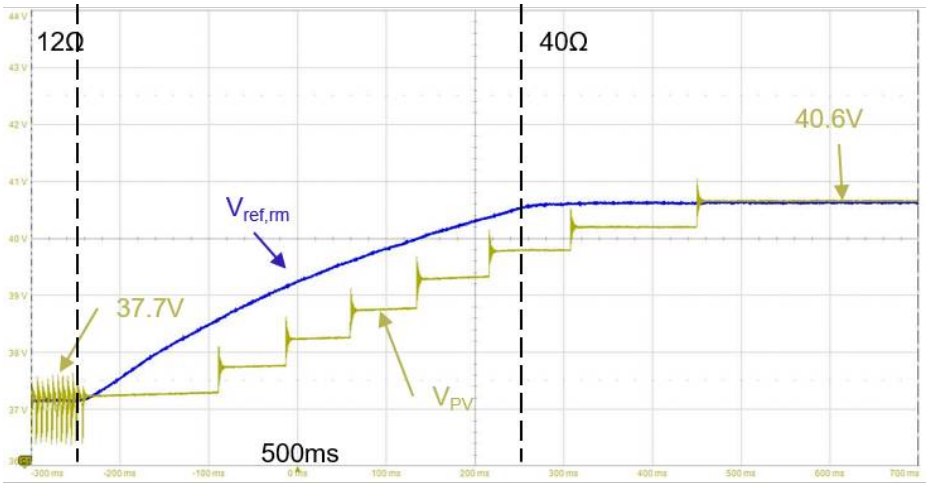
(b)

Figure 4-18: Experimental result of the hybrid controller ($1000W/m^2$, 25°C, linear load change $R_L = 40\Omega \leftrightarrow 12\Omega$) (a) Load decrement (b)Load increment

Hardware experiments were performed with a buck converter and a load resistor, as shown in Fig. 4-17. The outer control loop with the solar reference generator is implemented on the F28377S DSP board. Based on the unified control method, the experiment is conducted for the ramp load change. Two ramp patterns are tested. First, the load resistance started at 40Ω and decreased to 12Ω within 500ms, and secondly, the load resistance started at 12Ω and increased to 40Ω within 500ms. Such load patterns were created in the resistance sequence mode of the active load (Kikusui PLZ164W), and the DSP DA converter was used to observe the reference signal, which are internal variables of DSP. Fig. 4-18 shows the experimental waveform using the hybrid control method, and Fig. 4-19 shows the experimental waveform using the unified control method. In the hybrid control method, CS-VRC and RS-VRC references were observed and MRS-VRC reference was observed for



(a)



(b)

Figure 4-19: Experimental result of the unified controller ($1000W/m^2$, 25°C, linear load change $R_L = 40\Omega \leftrightarrow 12\Omega$) (a) Load decrement (b)Load increment

the unified control test. According to the hardware results, it is clearly observed that a reference level mismatch between two control region happens. Even though the simulations and hardware experiments show some differences due to noise and active load dynamics, these results prove that the unified method smoothly follows the I-V characteristic curve with higher speed than the hybrid scheme.

4.3 Fast reference generation

4.3.1 Conventional iteration algorithms

Mainly, three algorithms are considered in this study, and their behavior is briefly demonstrated in this section. The Lambert-Ω function is described in section 4.3.2 with more details.

4.3.1.1 Fixed point iteration

When the required function become

$$x = g(x), \tag{4.37}$$

the fixed point iteration can be written as

$$x_{n+1} = g(x_n), n = 1, 2, 3, ... \tag{4.38}$$

Here, note that the root α of the equation $x - g(x) = 0$ is a fixed point of the function g(x), meaning that α is a number for which $g(\alpha) = \alpha$

4.3.1.2 Newton-Raphson Method

If the required function is same as (4.37), the Newton-Raphson function can be written as

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}, n = 1, 2, 3, ... \tag{4.39}$$

It can be graphically demonstrated as shown in Fig. 4-20 The graphs of $f(x_n)$ and $f'(x_n)$ must contact, as seen on the graph and has at least one solution α for both graphs. By using this relationship, this method can be proved and described its different properties [94].

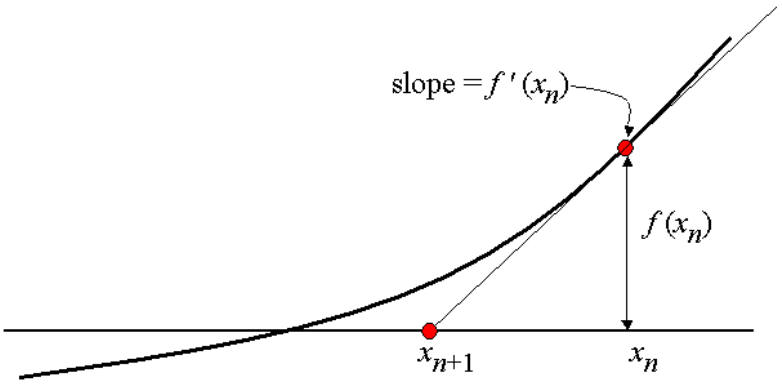


Figure 4-20: Graphical representation of Newton-Raphson method

Table 4.5: Parameters for PV module [9]

Parameter	KC200GT
$I_{sc}(A)$	8.21
$V_{oc}(V)$	32.9
$I_{mpp}(A)$	7.61
$V_{mpp}(V)$	26.3
N_s	54

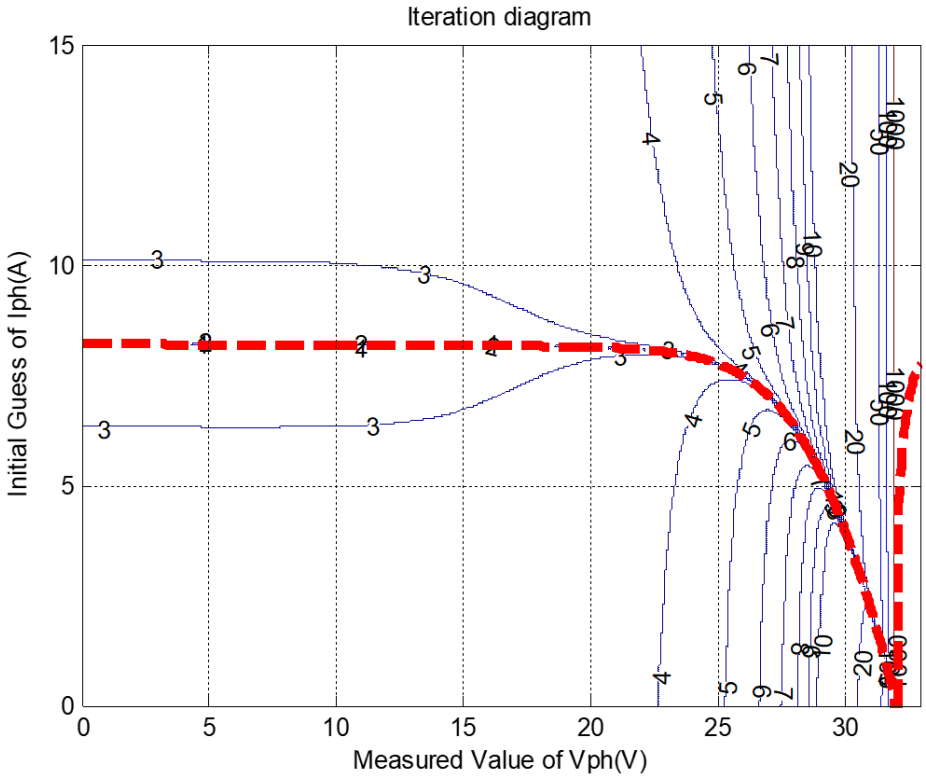
4.3.2 Approximated Lambert-Ω

4.3.2.1 Iteration number analysis of conventional methods

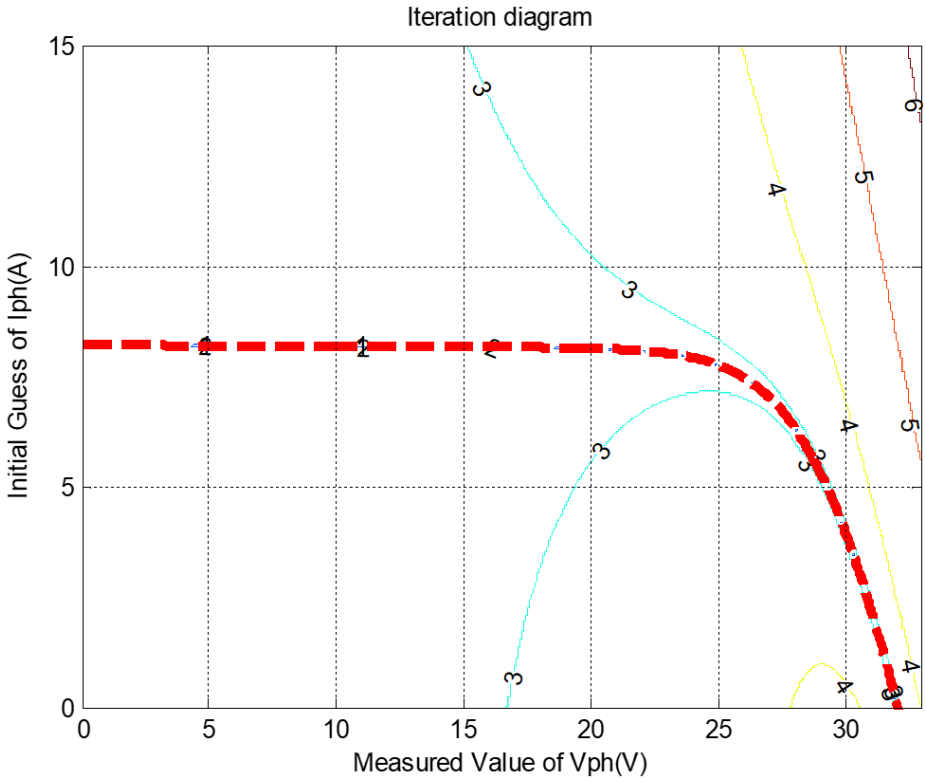
To examine the limitation of the conventional methods, two iterative algorithms in (1.10) and (1.11) are individually applied to the PV model of KC200GT in [95]. Table 4.5 summarizes the datasheet value and the model parameters of the PV sample. For fairness in comparison, the same stopping criterion,

$$|I_n - I_{n-1}| < 10^{-3} \tag{4.40}$$

has been tested for each algorithm and the maximum iteration limit is set to 1000. Iteration numbers are recorded for each algorithm according to various combinations of sensed voltage and initial guess of the solution and the results are plotted as a contour plot in Fig. 4-21. The labels on the plots indicate the iteration number required to meet the condition in 4.40. The red dotted thick line is the final solution calculated at the end of each algorithm. It is noted that the simple fixed-point iteration method in Fig. 4-21a requires larger number of iterations than the Newton's method does in Fig. 4-21b. Depending on the initial guess,



(a)



(b)

Figure 4-21: Iteration number diagram for conventional algorithms (a) Simple fixed-point iteration (b) Newton-Raphson method

the number of iterations may be dramatically increased and, in some cases, the final value may not converge to a correct value even with 1000 iterations.

4.3.2.2 Derivation of the explicit forms of the PV model equation

Conventional PV model reference generation requires considerable computational power. To avoid such a computational burden, the lookup table-based SAS system was implemented [18, 22, 27–30, 33–35]. Some commercialized SAS systems used this method to save computational power and maintain the simplicity of the algorithm. However, it consumes a large storage capacity, and accuracy depends on the data harvesting method and resolution of the lookup table.

Thus, a reference generation technique that has less computational power and less storage capacity is required. As a solution, many approximation techniques are proposed to manipulate the PV equation. Then the accuracy will be comparatively reduced, but it will sufficiently satisfy the industrial standards. As one example, Lambert-Ω-function was implemented. To solve the implicit model equation without iteration, it is convenient to use the inverse function $\Omega(x)$ of the form

$$\Omega(x)e^{\Omega(x)} = x. \tag{4.41}$$

Mathematically, it is well known and is referred to as the Lambert-Ω function or the Omega function and has been applied to many practical fields [96, 97]. The Lambert-Ω function derives the inverse form for the PV model equation. The PV equation can be converted either in voltage form or current form, and such a derivation is explained using the appropriate circuit simplification of the single-diode equivalent circuit in Fig. 1-7c.

First of all, the PV equivalent circuit model can be simplified by Thevenin transformation as shown in Fig. 4-22a. In this voltage form, the diode current is given by

$$I_D + I_O = I_O e^{\frac{\frac{vR_{sh}}{R_{sh}+R_s}+(I_{ph}+I_D)(R_{sh}||R_s)}{ANV_t}} \tag{4.42}$$

By separation of the diode current and the terminal voltage into the opposite side, we obtain

$$\frac{(I_D+I_O)(R_{sh}||R_s)}{ANV_t} e^{\frac{(I_D+I_O)(R_{sh}||R_s)}{ANV_t}} = I_O \frac{R_{sh}||R_s}{ANV_t} e^{\frac{vR_{sh}+(I_{ph}+I_O)R_{sh}R_s}{ANV_t(R_{sh}+R_s)}} \tag{4.43}$$

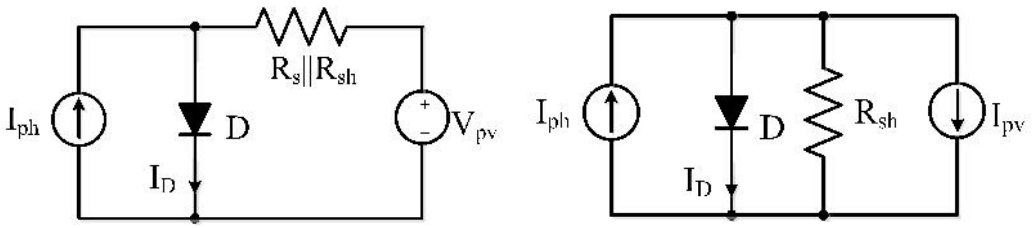


Figure 4-22: Simplification of the PV circuit model to use Lambert-Ω form (a) The terminal voltage as an independent variable (b) The terminal current as an independent variable

Comparing (4.41) and (4.43), the following holds.

$$\frac{(I_D + I_O)(R_{sh}||R_s)}{ANV_t} = \Omega\left[I_O\frac{R_{sh}||R_s}{ANV_t}e^{\frac{vR_{sh}+(I_{ph}+I_O)R_{sh}R_s}{ANV_t(R_{sh}+R_s)}}\right] \tag{4.44}$$

Therefore, the diode current can be only described by the terminal voltage as

$$I_D = \frac{ANV_t}{R_{sh}||R_s}\Omega\left[I_O\frac{R_{sh}||R_s}{ANV_t}e^{\frac{vR_{sh}+(I_{ph}+I_O)R_{sh}R_s}{ANV_t(R_{sh}+R_s)}}\right] - I_O \tag{4.45}$$

Since the terminal current is related to the diode current by

$$i = I_{ph} - I_D - \frac{(v+IR)}{R_{sh}}, \tag{4.46}$$

the terminal current is explicitly determined from the terminal voltage as follows:

$$i = \frac{(I_{ph}+I_O)R_{sh} - v}{R_{sh}+R_s} - \frac{ANV_t}{R_s}\Omega\left[\frac{I_O(R_{sh}||R_s)}{ANV_t}e^{\left(\frac{vR_{sh}+(I_{ph}+I_O)R_{sh}R_s}{ANV_t(R_{sh}+R_s)}\right)}\right] \tag{4.47}$$

On the other hand, the current form can be derived by Norton transformation as in Fig. 4-22b. The diode current is given by

$$I_D + I_O = I_O e^{\frac{(I_{ph}-I_D-i)R_{sh}}{NV_t}}. \tag{4.48}$$

By separation of the diode current and the terminal current into the opposite side, we obtain

$$\frac{(I_D+I_O)R_{sh}}{NV_t}e^{\frac{(I_D+I_O)R_{sh}}{NV_t}} = \frac{I_O R_{sh}}{NV_t}e^{\frac{(Iph-I_O-i)R_{sh}}{NV_t}}. \tag{4.49}$$

Therefore, comparing 4.41 and 4.49, the following holds.

$$\frac{(I_D + I_O)R_{sh}}{NV_t} = \Omega\left[\frac{I_O R_{sh}}{NV_t} e^{\frac{(Iph - I_O - i)R_{sh}}{NV_t}}\right] \tag{4.50}$$

Consequently, the terminal voltage is explicitly determined from the terminal current as follows:

$$v = -i(R_{sh} + R_s) + I_{ph}R_{sh} - NV_t\Omega\left[\frac{I_O R_{sh}}{NV_t} e^{\frac{(Iph - I_O - i)R_{sh}}{NV_t}}\right] \tag{4.51}$$

4.3.2.3 Non-iterative evaluation of the Lambert-Ω function

Eqs. 4.47 and 4.51 are the explicit counterparts of the PV model equation. Because it implicitly has been removed, they can be used for a direct calculation of the operating points - the current from the sensed voltage by 4.47, or the voltage from the sensed current by 4.51. However, a problem still exists: to calculate the value of Ω(x) for an arbitrary x. Because the Lambert-Ω function itself is defined recursively, most software packages provide a dedicated function implementation such as 'lambertW(x)' in MATLAB, in Maple, 'ProductLog[x]' in Mathematica. Sometimes, it can be evaluated by an additional iteration method. It can be regarded that nothing has been changed because the mathematical implicitly has not been removed but just moved from the model equation into the Ω-function.

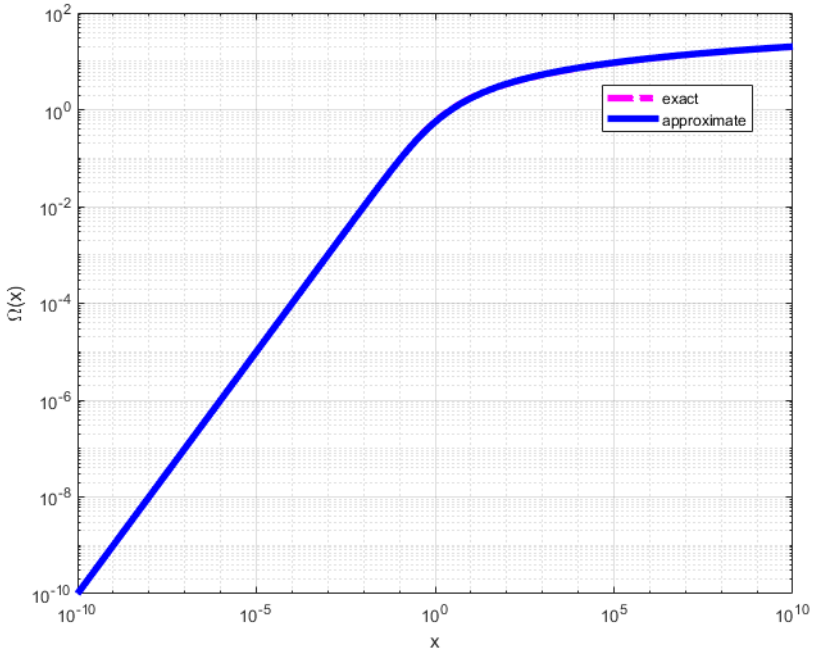
However, in order to avoid such an iteration, there has been numerous studies on analytic approximation techniques for the Ω-function [98]. One of the most useful approximation is the form presented by Winitzki [99] given as

$$\Omega(x) = ln(1+x)\left[\frac{1 - ln(1 + ln(1+x))}{2 + ln(1+x)}\right] \tag{4.52}$$

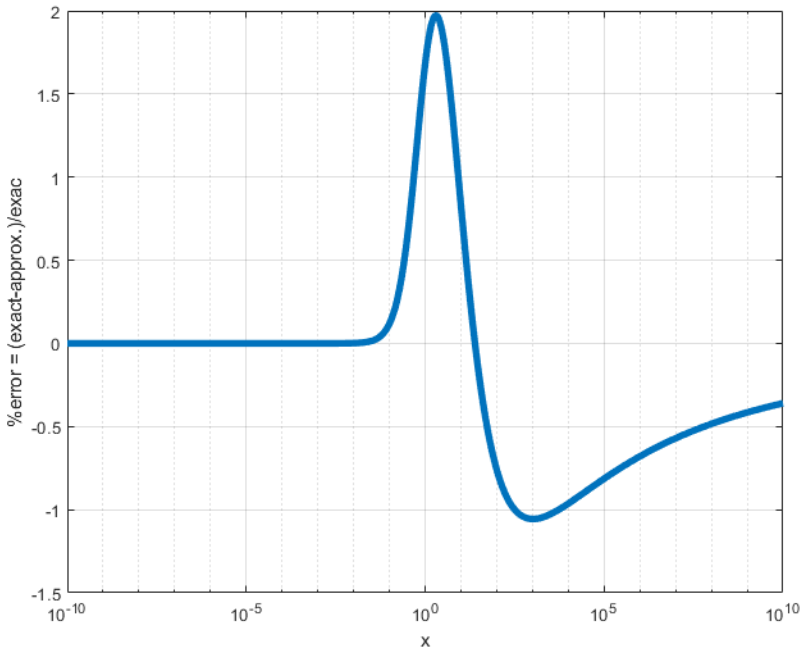
where x is real and non-negative number. Fig. 4-23 shows the accuracy and the error caused by this approximation for a wide span of x values. The worst-case error is less than 2% and it proves the validity of this approximation. By combining (4.52) with the two explicit forms just derived in (4.47) and (4.51), a powerful and computationally efficient algorithm to generate PV characteristics can be obtained, which is the proposed method of this study.

4.3.2.4 Performance comparisons

Using the proposed method together with conventional ones, the I-V curve generation is performed, and the results are compared in Fig. 4-24a. Every algorithm works well and shows almost the same results except that the simple fixed-point iteration method showing a few incorrect results near the open circuit voltages. Fig. 4-24b shows the average CPU

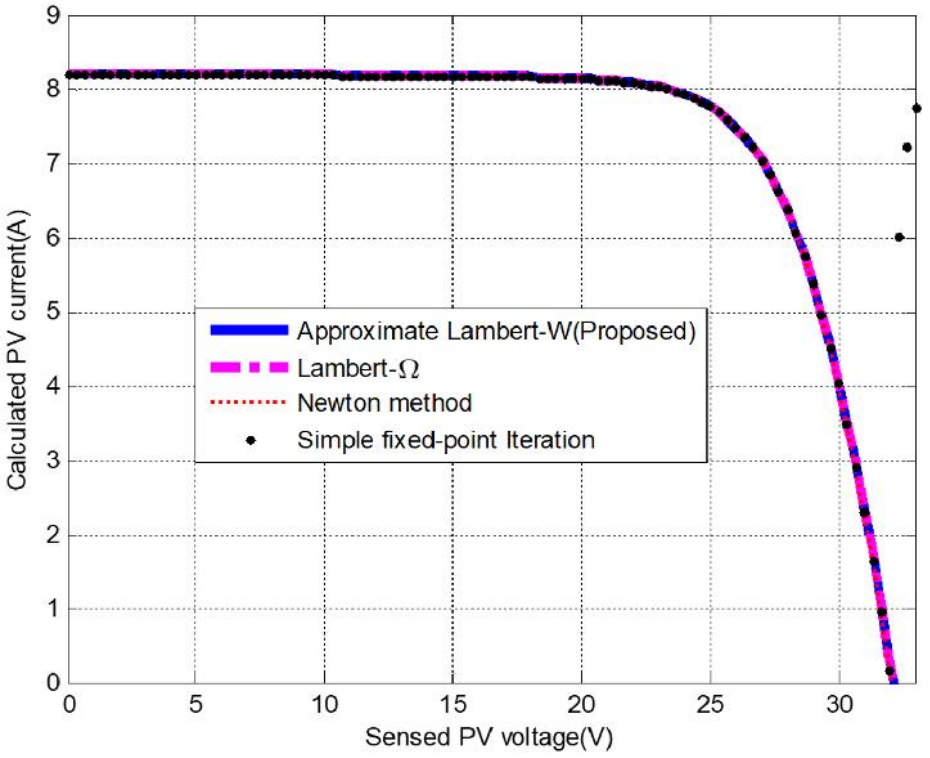


(a)

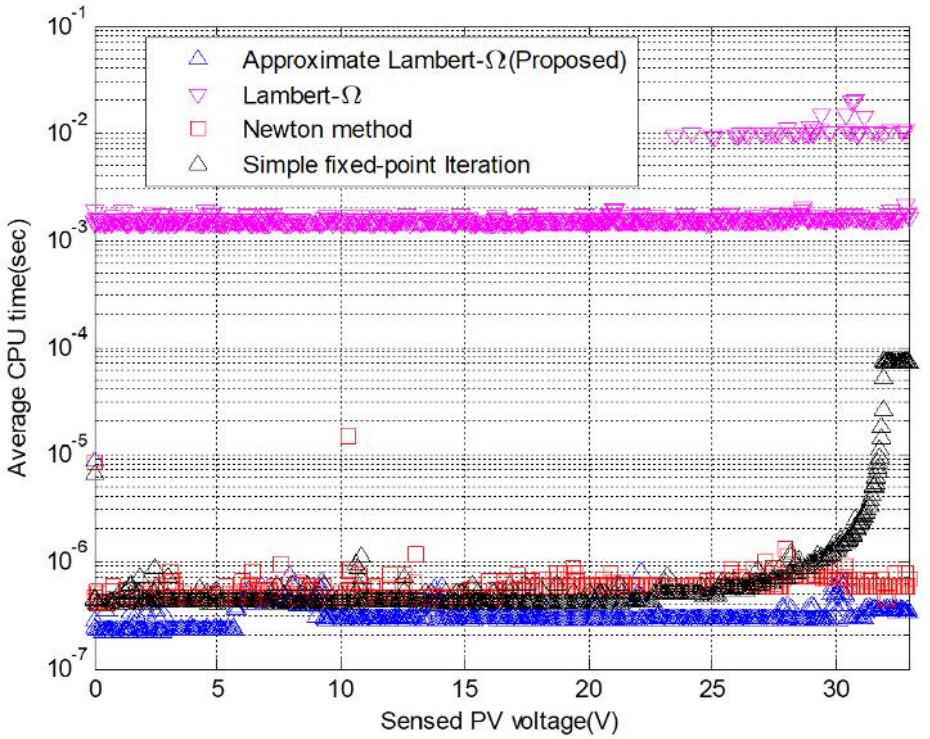


(b)

Figure 4-23: Analytical approximation of the Lambert-Ω function (a) Behavior against the voltage (b) Error presentage



(a)



(b)

Figure 4-24: Simplification of the PV circuit model to use Lambert-Ω form (a) I-V curve generation (b) Average CPU time for 100 repeated executions

Table 4.6: PV module Parameters of performance comparison

Parameter	KC200GT	KC65GT	MSX120	SQ-160-PC
$I_{sc}(A)$	8.21	3.99	3.87	4.9
$V_{oc}(V)$	32.9	21.7	42.1	43.5
$I_{mpp}(A)$	7.61	3.75	3.56	4.58
$V_{mpp}(V)$	26.3	17.4	33.7	35
N_s	54	36	72	72

time measured by MATLAB R2013a (32-bit) under a PC platform: 3.40GHz Intel Core i7 CPU. To measure the CPU time, each function is executed 100 repeated times and the total CPU time is accumulated and averaged.

The simple fixed-point iteration method shows a wide variety of calculation time, and the time dramatically increases as the operating point approaches the open-circuit voltage. Newton's method shows about 0.4 0.6 micro-seconds and shows a slight increase in the CPU time beyond the maximum power point. It is also noticeable that the Lambert-Ω function implementation in MATLAB, 'lambertW(x,0)', shows a surprisingly slow performance of more than a few milliseconds to be caused by the internal recursion mentioned above. On the contrary, the proposed method shows 0.2 0.3 micro-sec consistently. Even though the absolute CPU time is highly dependent on computing environments and thus is of less importance, a relative comparison of the execution time concludes that the proposed method is superior to other methods because it increases calculation speed by more than 30% on average and shows very stable calculation time irrespective of the operating point.

4.3.3 Super-ellipse Approximation

As an explicit PV generator model, a super-ellipse approximated PV model can be introduced for the SAS scheme. In the scope of the stability, it also shows the nullification of the outer loop as discussed in Chapter-2 and 3. Here, the validity of this method is confirmed. The four different commercial PV modules in Table 4.6 are used to compare the super-elliptical approximation curve and conventional single-diode model from the perspective of the accuracy in the V_{mpp}, I_{mpp}, and P_{mpp}. Each curve are generated on MATLAB and shown in Fig. 4-25. The order of the super-ellipse can be calculated by Algorithm 1. It is converged into the final value as shown in Fig. 4-26.

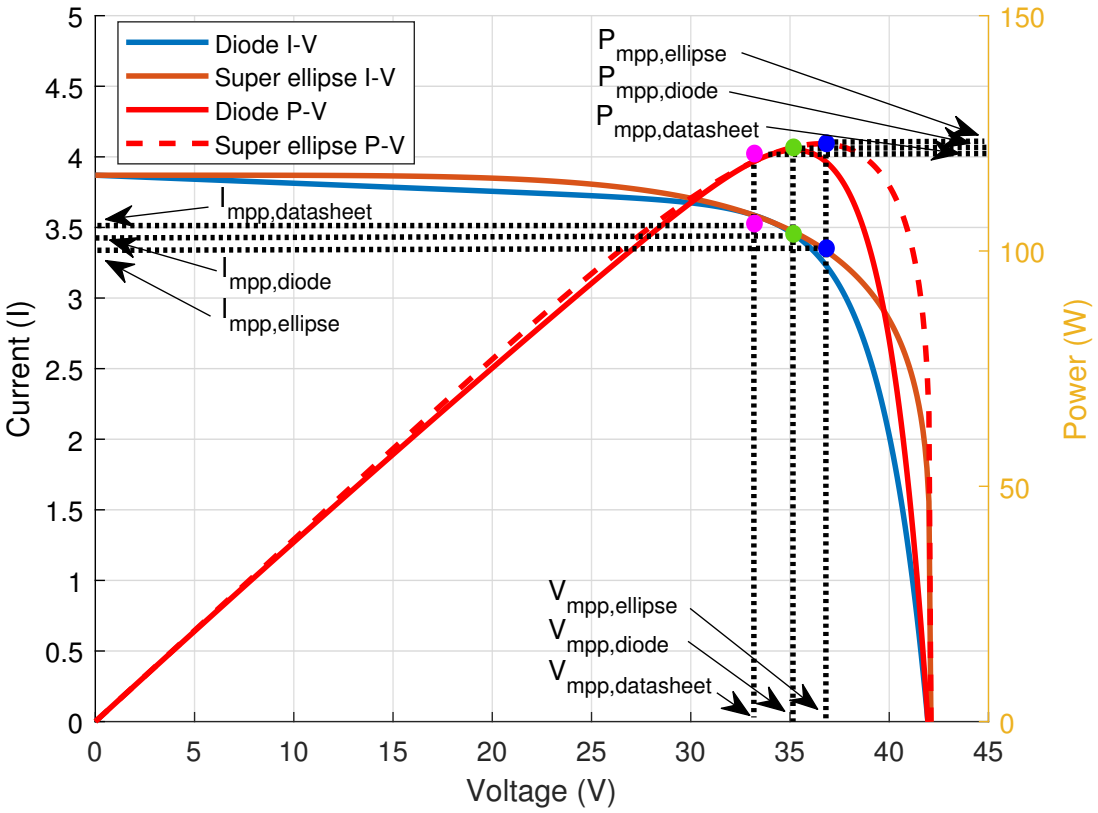


Figure 4-25: Behavior of SAS duty and critical duty of CCM boundary condition vs load resistance

```
clear;
clc;
width = 3;
size = 12;
Imp=3.57;
Vmp=33.7;
Iscn=3.87;
Vocn=42.15;
A = Vmp/Vocn;
B = Imp/Iscn;
i = 1;
for i = 2:30
N(1,i) = - B^(N(1,i-1))/log(A/B);
end
```

Algorithm 1: Order of super-ellipse

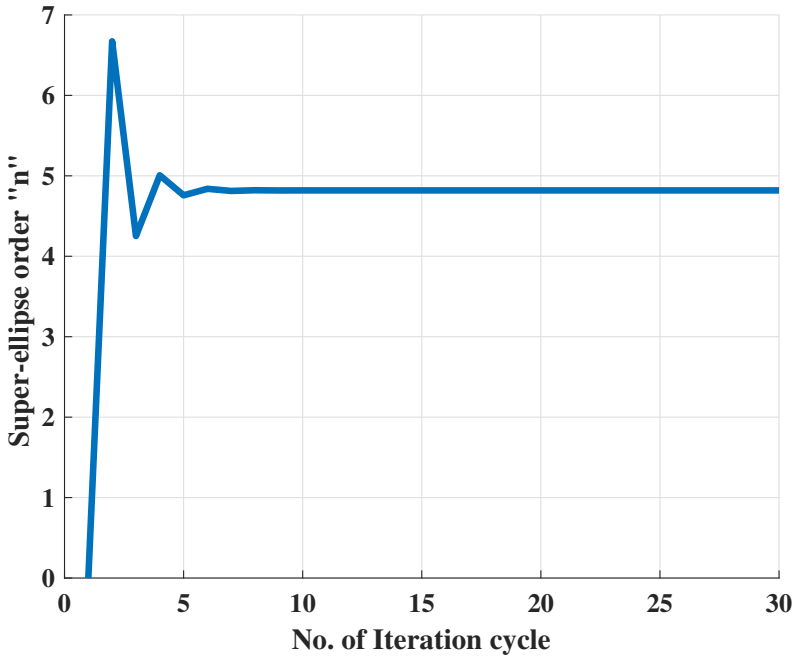


Figure 4-26: Manipulation of super-ellipse order (MSX120)

The observations were noted in Table 4.7. The super-elliptical model has slightly higher error of 4%, which is just half (2%) of the diode model. It looks the accuracy is quite acceptable SAS response.

4.4 Speed enhancement of controller

4.4.1 Limitation of the conventional buck converter

Unlike the conventional adjustable supply, the SAS system should provide the fast dynamic voltage and current. To achieve this requirement, the output capacitor makes a dilemma because it provides the low voltage ripple in the output but hinders a rapid decrement of the output voltage. [100] demonstrates this issue. According to Fig. 4-27, the rising edge slew rate becomes 36mV/μs, but in the falling edge, it is only under 32mV/μs slew rate due to RC discharge time constant.

To address this issue, the bidirectional converter topology should be adapted.

4.4.2 Adoption of the synchronous buck converter

The schematic of the converter is shown in Fig.4-28. To modify the conventional buck into a synchronous buck converter, the freewheeling diode is replaced with a MOSFET.

Table 4.7: Comparison of super ellipse parameters

PV brand	PV model	order n	P_{mpp} (W)	Error %	I_{mpp} (A)	Error %	V_{mpp} (V)	Error %
MSX 120	Datasheet		120		3.56		33.7	
	Single diode model		121.45	1.21	3.45	3.19	35.2	-4.26
	Super elliptical model	4.9	122.78	2.32	3.35	6.27	36.6	-7.92
KC 65GT	Datasheet		65		3.75		17.4	
	Single diode model		65.95	1.46	3.6	4.17	18.3	-4.92
	Super elliptical model	5.6	67.6	4	3.52	6.53	19.2	-9.37
KC 200GT	Datasheet		200		7.61		26.3	
	Single diode model		203	1.5	7.33	3.82	27.7	-5.05
	Super elliptical model	5.1	205.81	2.90	7.15	6.43	28.8	-8.68
SQ 160-PC	Datasheet		160		4.58		35	
	Single diode model		162.01	1.26	4.43	3.39	36.6	-4.37
	Super elliptical model	5.4	164.89	3.06	4.31	6.26	38.3	-8.62

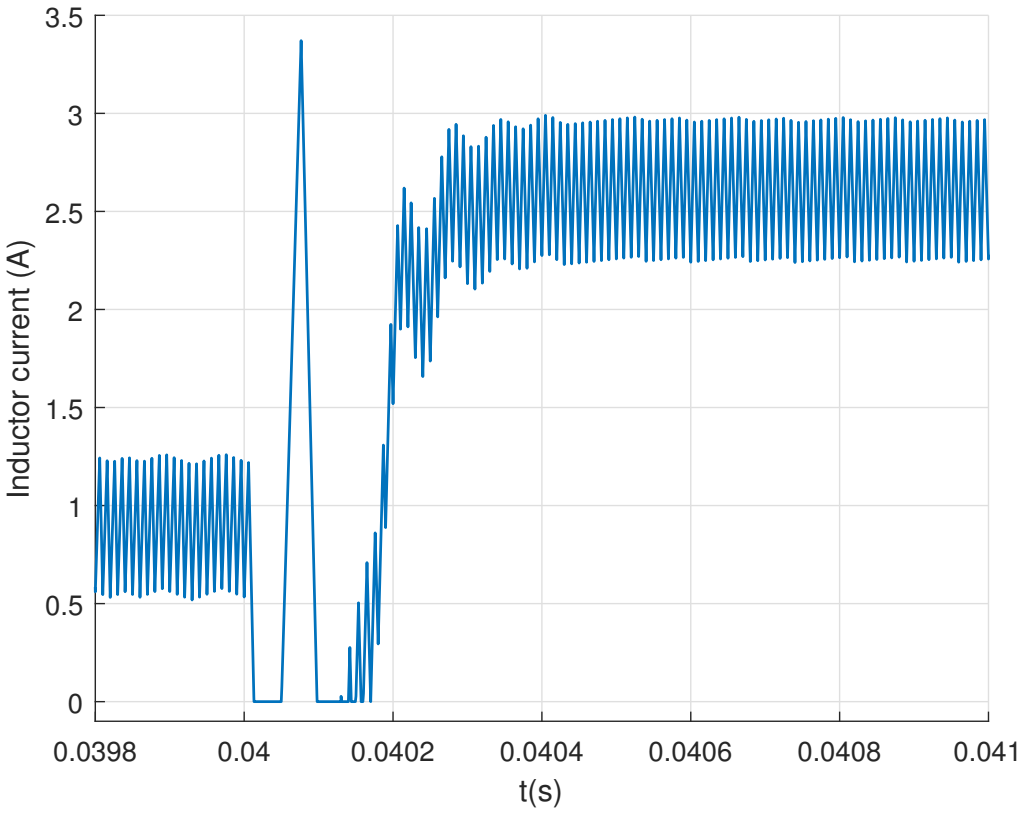


Figure 4-27: Inductor current of buck converter

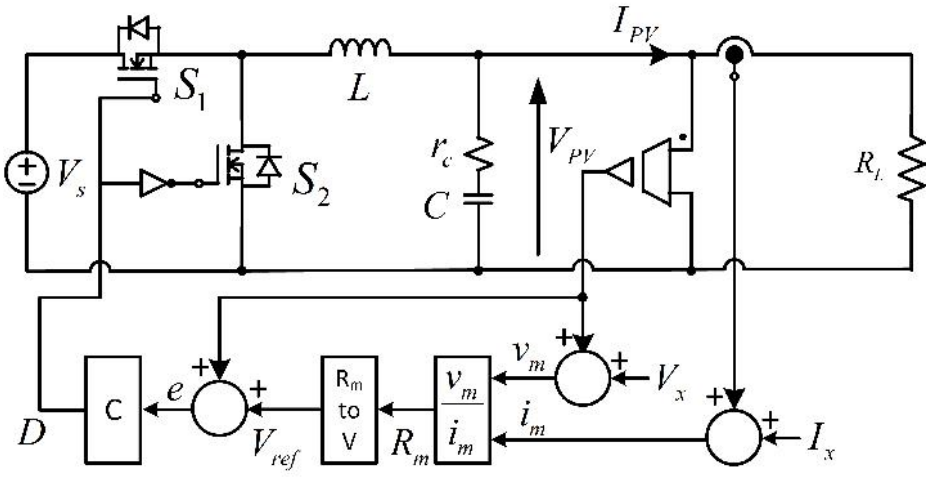


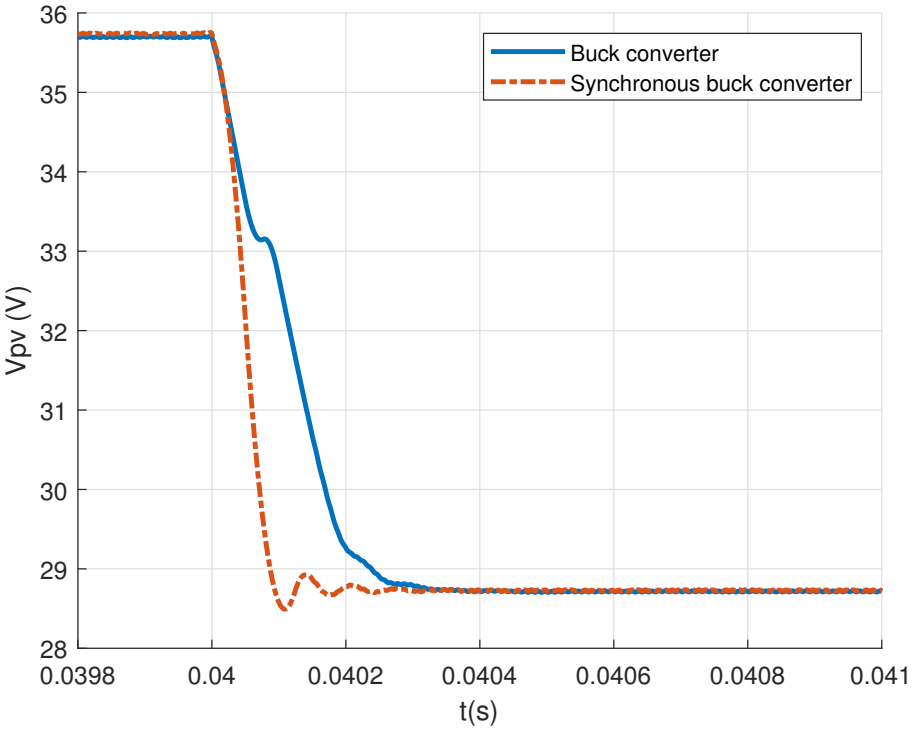
Figure 4-28: Simulation schematic

Considering the performance of the body diode, the MOSFET (FDP150N10) was selected, which has a low body diode reverse recovery time (t_{rr}). Buck and synchronous operation can be interchanged by activating the low side gate driver input in this structure.

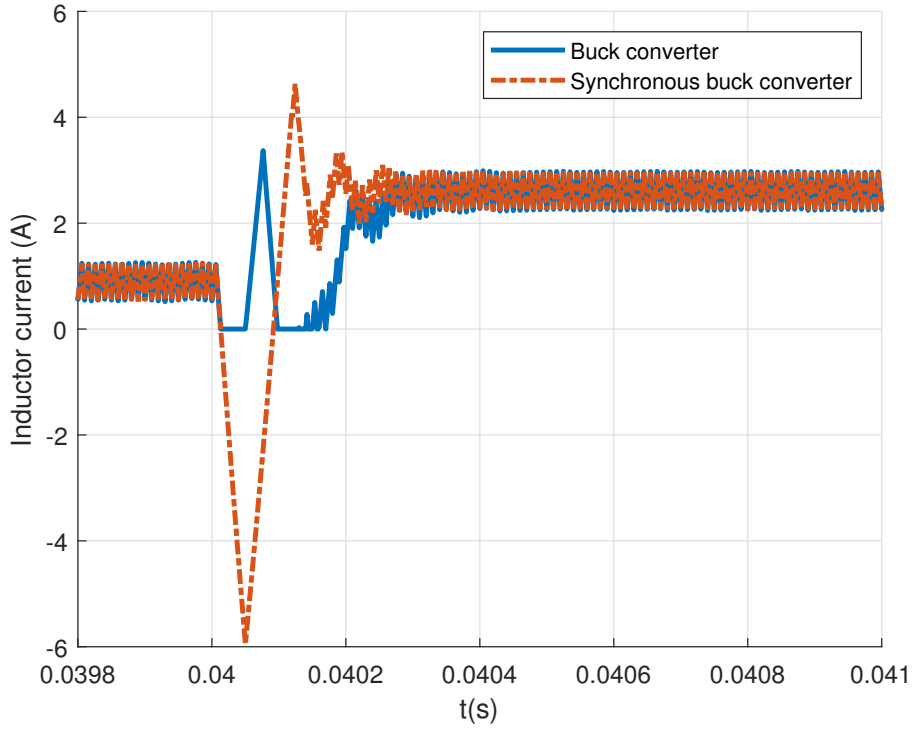
In the synchronous buck power stage, the test is newly set up by using RS-CRC 11Ω ↔ 40Ω as shown in Fig. 4-29 which has an increment and decrement of resistance to compare the performance. According to this figure, the synchronous buck converter shows higher slew rate in both rising edge and falling edge, which is 36mV/μs and 72mV/μs, respectively. The inductor current as shown in Fig. 4-27 clearly demonstrate that buck converter enters to the DCM mode on the load change instant and follows the RC time constant curve, but synchronous buck can flow the negative current in the inductor as shown in Fig. 4-29 and quickly discharge the output capacitor. In this test, controller which is used for small-signal analysis is re-used to keep maintain the same controller performance. The wave forms of the load transient are shown in Fig. 4-30. However, synchronous buck converter shows comparatively higher slew rate, thus controller is re-designed to have optimum response.

4.5 Conclusion

In this chapter, proposed advanced SAS control strategies were demonstrated. First, the unified control strategy is introduced to solve the control mode switching problem of the hybrid method. As two available hardware configurations, MRS-VRC and MRS-CRC methods are presented. The stability analysis shows that both methods nullify the reference generator dynamics, and the requirement for the projected origin (V_x, I_x) is also demonstrated. The



(a)



(b)

Figure 4-29: Step load change $11\Omega \leftrightarrow 40\Omega$ of RS-CRC system in buck and synchronous buck converter (a) V_{PV} (b)Inductor current

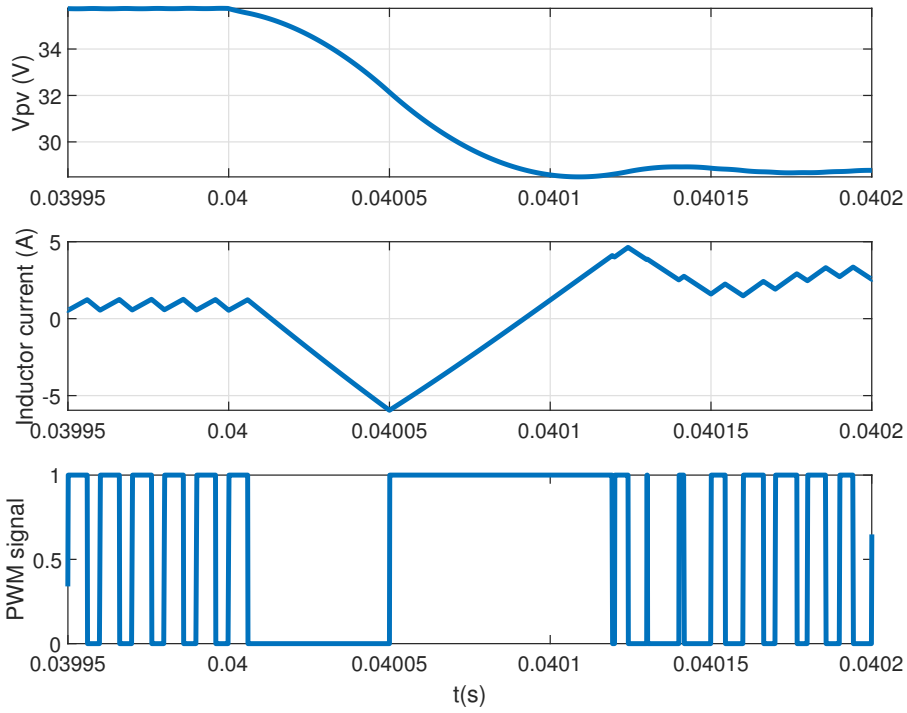


Figure 4-30: Synchronous buck converter wave forms of the load transient

simulation and experiment results show that a unified controller can mitigate the limitation of the hybrid system.

As a fast convergence of SAS reference generation, the Lambert-Ω method is demonstrated to eliminate the implicitness of the PV equation. First, the single-diode PV model was adopted into the Lambert-Ω function, presenting a non-iterative approximation. Then the error and iteration numbers are compared with conventional iteration methods. The accuracy and average CPU cycle time diagrams explain the superiority of approximated Lambert-Ω method.

For more simple reference generation, the super-ellipse approximation is proposed. Here, the MPP location is generated by a conventional single-diode PV model, and the super-elliptic PV model is compared by using four commercial PV modules. The errors in P_{mpp}, I_{mpp}, and V_{mpp} are observed. As a result, a simple and fast convergent method, the super-elliptic PV model, is proven to be suitable for fast dynamic PV emulations.

Finally, the hardware limitation of the conventional power stage is studied. It is found that the DCM operation in the low output current condition makes a performance degradation. It increased the output ripple and slowed down the system response in voltage

decrement instant. Thus, the bidirectional topology is recommended for the SAS power stage. In a test by synchronous buck converter, the proposed converter stage shows a comparatively higher slew rate than the conventional uni-directional converter.

Chapter 5

Conclusion and future works

5.1 Conclusion

In this study, small-signal modeling and analysis were carried out to express the entire solar panel simulation system. Although many researchers have worked on PV models, articulating its design and interaction with MPPT control, the stability of the SAS internal structure remained relatively untouched due to its complex mathematical equations and analysis required, making it complicated. To simplify the analysis of the SAS, a mathematically simplified and parameter-wise PV characteristic compatible approximate model is required. The super elliptic function became the best option because it can satisfy the main three points V_{oc}, I_{sc}, MPP of the PV characteristic curve. Thus, the elliptical curve was used in this paper because its gradient spread zero to infinity and satisfied all possible gradients.

From the control loop analysis, this study demonstrated that SAS is inherently a multi-loop system consisting of the inner control loop and the outer reference generation loop. It is found that the two loops interact with each other according to the operating points, and the degree of interactions appear in various patterns according to the control architecture. The dynamic stabilities of the CS-VRC, VS-CRC, RS-VRC and RS-CRC configurations were analyzed and compared. Resistance sensing methods can nullify the outer loop dynamics, which started from the PV reference generator. Primarily, the RS-VRC configuration was more robust to the operating point change than other methods, which were cross-validated through simulations and experiments. The proposed approach and accompanying results are expected to be helpful for the control performance enhancement of SAS systems.

Besides, the three-section hybrid SAS controller was implemented to answer the draw-

back of the two-section hybrid control system. The third section was introduced to cover the vicinity of MPP, and load resistance was utilized by using current and voltage sensing information. It improves the performance, which enhances the accuracy of the conventional hybrid system. However, a hybrid system also has another drawback in the control mode transition. When the control loop changes in the hybrid system, it generates a slight fluctuation in the output voltage due to a mismatch of two reference signals. It will affect the MPPT algorithm and efficiency test procedures of MPPT controllers. Thus, a unified control schema is motivated.

The resistor sensing method is suitable for a unified SAS control, but it has a limitation near the V_{oc}. Because the PV current is close to zero and it makes an immense resistance value close to infinity. With the measurement noise, if the current sensing value becomes hard to be different from the noise level. A unified control scheme called MRS-VRC was proposed to address this issue by shifting the origin of the measurement point by adding fixed voltage and current (V_{oc}, I_{sc}) into sensing signals. Two approaches are proposed to inject this offset value which is introduced as soft injection and hard injection. The soft injection method can easily implement because the modification is made only in the algorithm. However, it cannot improve the hardware limitations. On the contrary, the hard injection can mitigate the hardware limitation. However, the modified resistance is calculated in both cases, and the modified resistance to the reference voltage is used for reference generation. Simulation and experiment results were also verified that a hybrid system has a mismatch in the reference signals of each control region, while a unified control method can eliminate such drawbacks.

To obtain a more accurate explicit PV model, an approximated Lambert-Ω function is proposed. It is compared with a conventional numerical method such as fixed-point iteration, Newton-Rapson method, and Lambert-Ω function, which is used to manipulate the implicit PV reference generation. The proposed approximated Lambert-Ω function shows acceptable accuracy for the PV reference generation and enormous reduction of CPU calculation time. Thus, this method provides a promising SAS performance in the micro-controller level SAS implementation.

By using the small-signal analysis, the proposed unified control method is analyzed with some modifications. The developed small-signal analysis verified it. The best selection for the offset current and voltage is proposed by analyzing the system stability. It has considered the hardware limitation to obtain the V_{oc} and I_{sc} condition. The V_x and I_x are determined by considering the minimum hardware duty ratio requirement and boundary conditions for

converter DCM boundary conditions.

The hardware limitation SAS makes a severe impact on system performance. The output capacitor makes an unnecessary delay when the output voltage decrement. Thus, the bi-directional DC-DC converter is introduced to the SAS scheme. As a simple implementation of this concept, the synchronous buck topology is used, and it provided several advantages such as faster voltage decrement performance and DCM elimination. Due to compatibility for the negative current of this topology, the SAS scheme can be extended into the fourth quadrant operation in the future.

Finally, this study is useful to understand the modeling and stability of the SAS and the limitation of the SAS model and power stage. Each of the issues is clearly addressed, and possible solutions are given. A few more studies are identified and made definitions to continue more research in the future.

5.2 Future Works

According to the development of new features of the SAS, it has several extensions for future research. Following research directions can be identified from this study.

- The unified controller with hard injection is needed to be developed to maximize the operating range of the SAS further. V_x and I_x can be developed as an input regulated DC/DC converter, and its output power can be fed back to the converter power as a regenerative power.

- The dynamic of the reference generator can be extended as an insolation and temperature disturbance system. According to the SAS topology and load configuration, this effect can be changed, and time delay also relates to the reference generation. Thus, more researches are needed to get a conclusion about time delay, insolation, and temperature.

- Generally, most commercial SAS is designed for first quadrant I-V curve operation by adding an un-removable parallel diode into the SAS output. Thus, the bidirectional converter should be improved for covering the second and fourth quadrant of the IV curve. Then, the PV cell level emulation will be possible.

- Although the MPPT controller is not much discussed in this thesis, most of the analysis-based studies were continued in this area. The influence of sampling time

for MPPT and SAS is not touched often, and it is essential to improve the SAS performance furthermore. Accordingly, the stability limitations for partial shading conditions should be studied.

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